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0062F0 2H626H60

FIG. 1

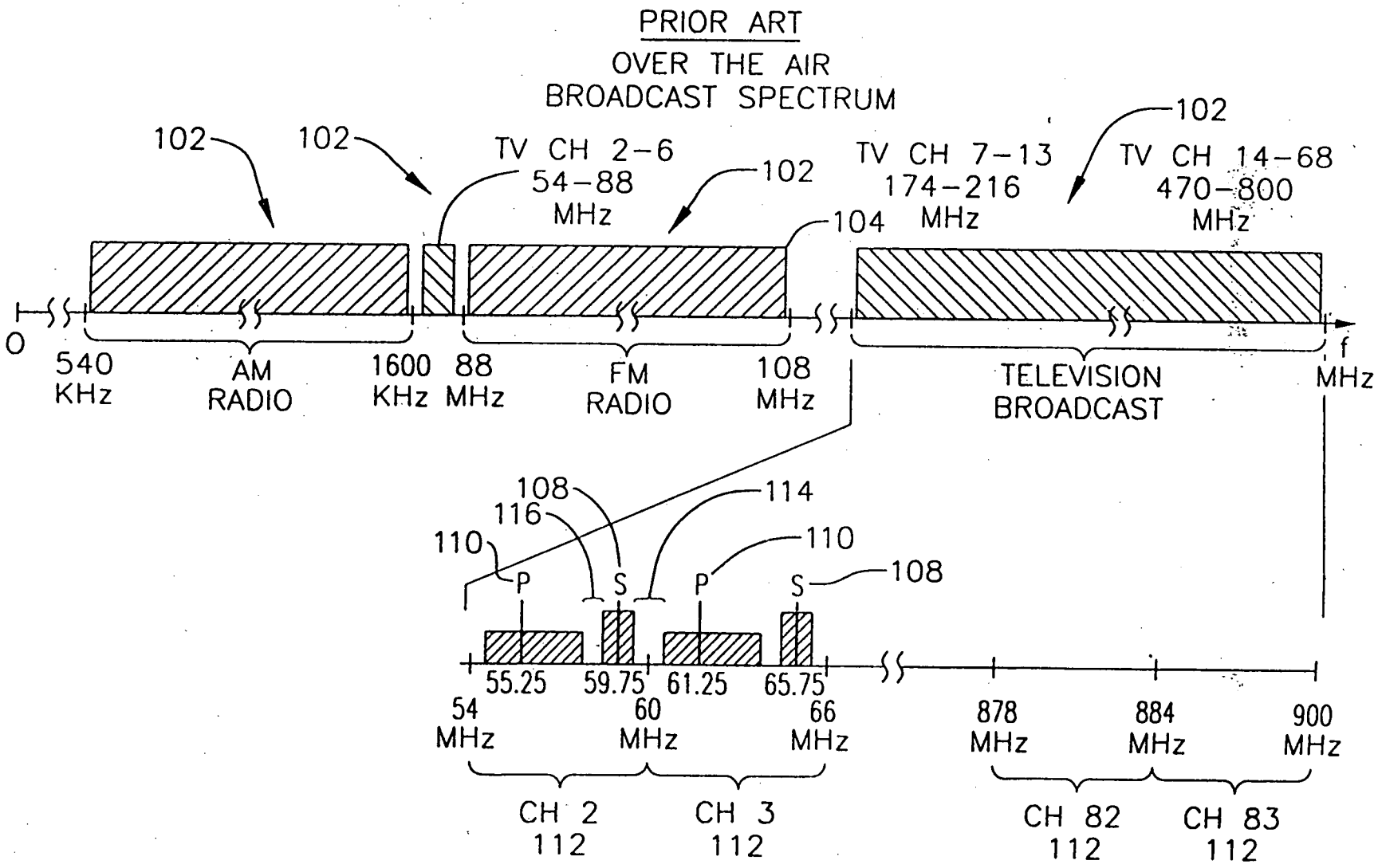


FIG.2

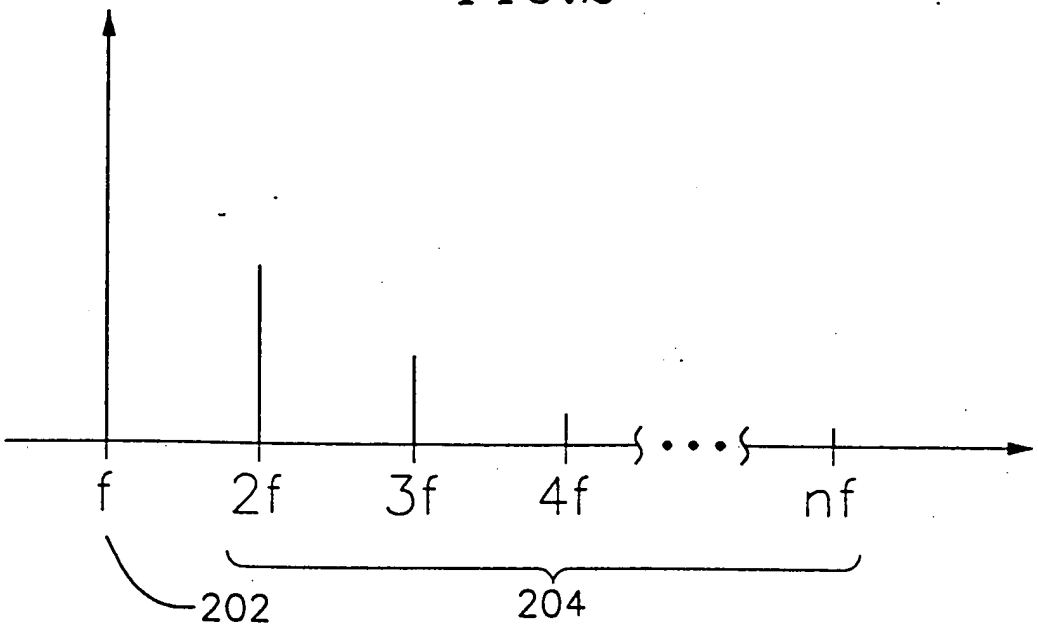
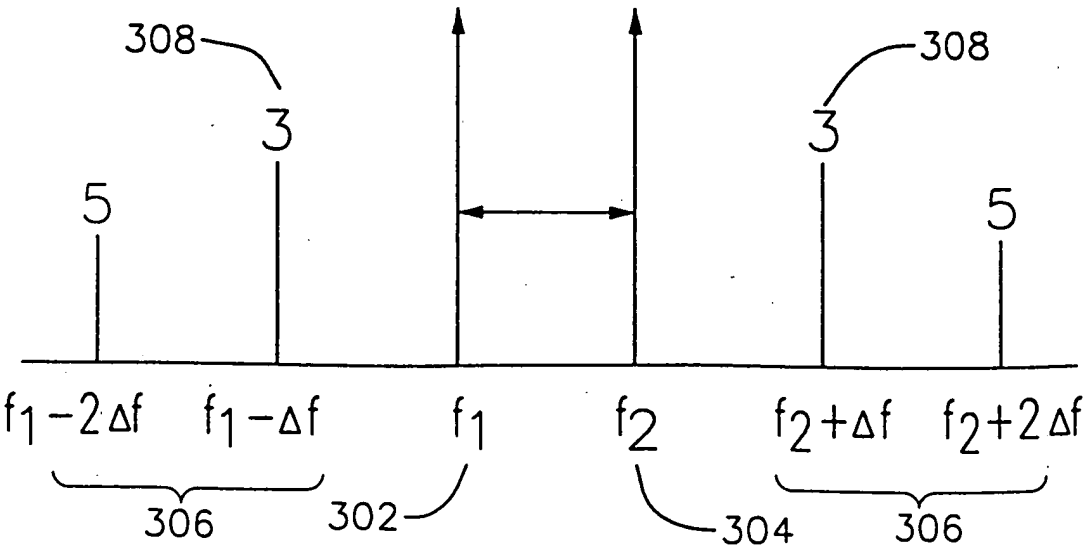
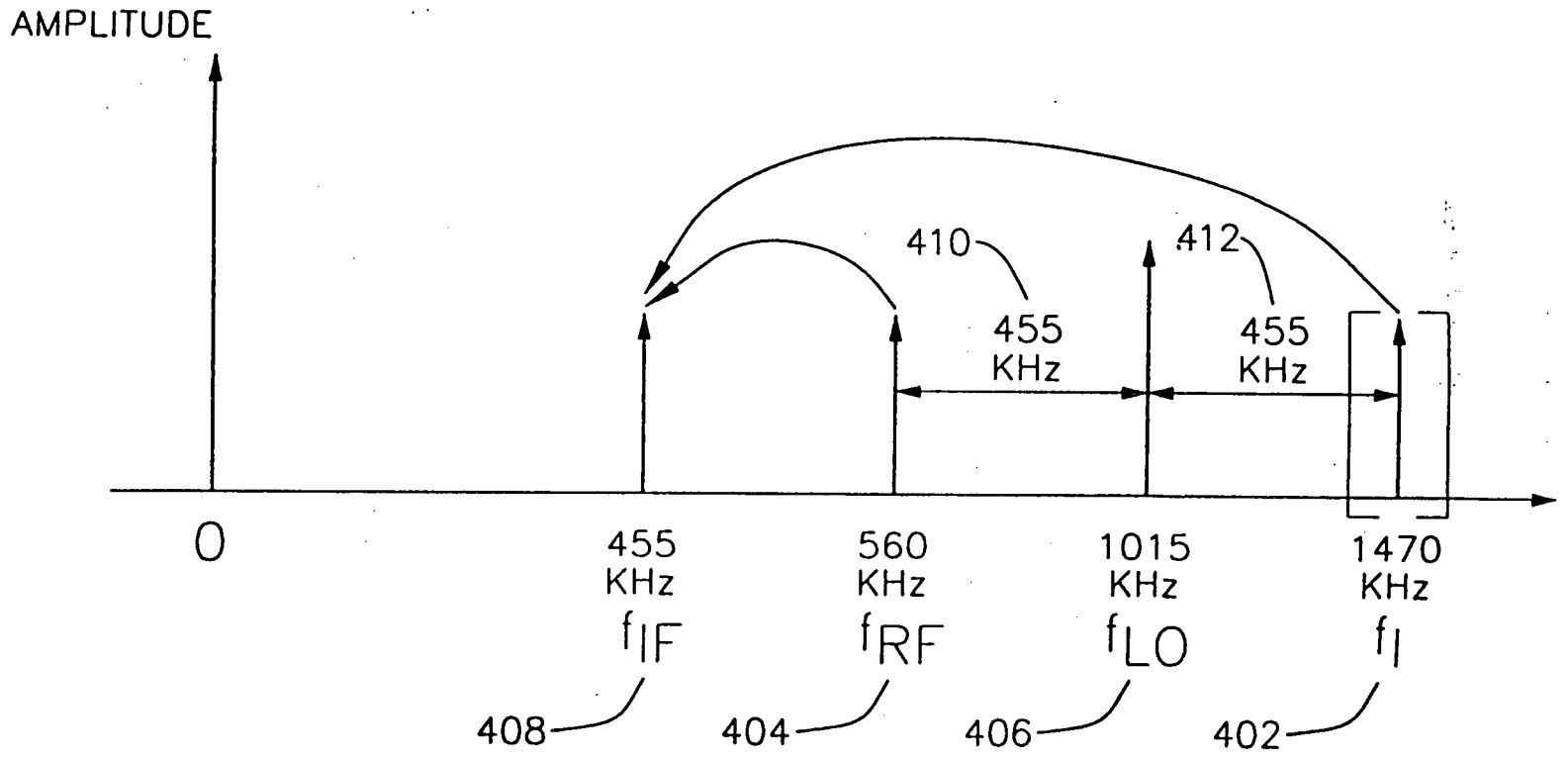


FIG.3
PRIOR ART



08270 2A626A0

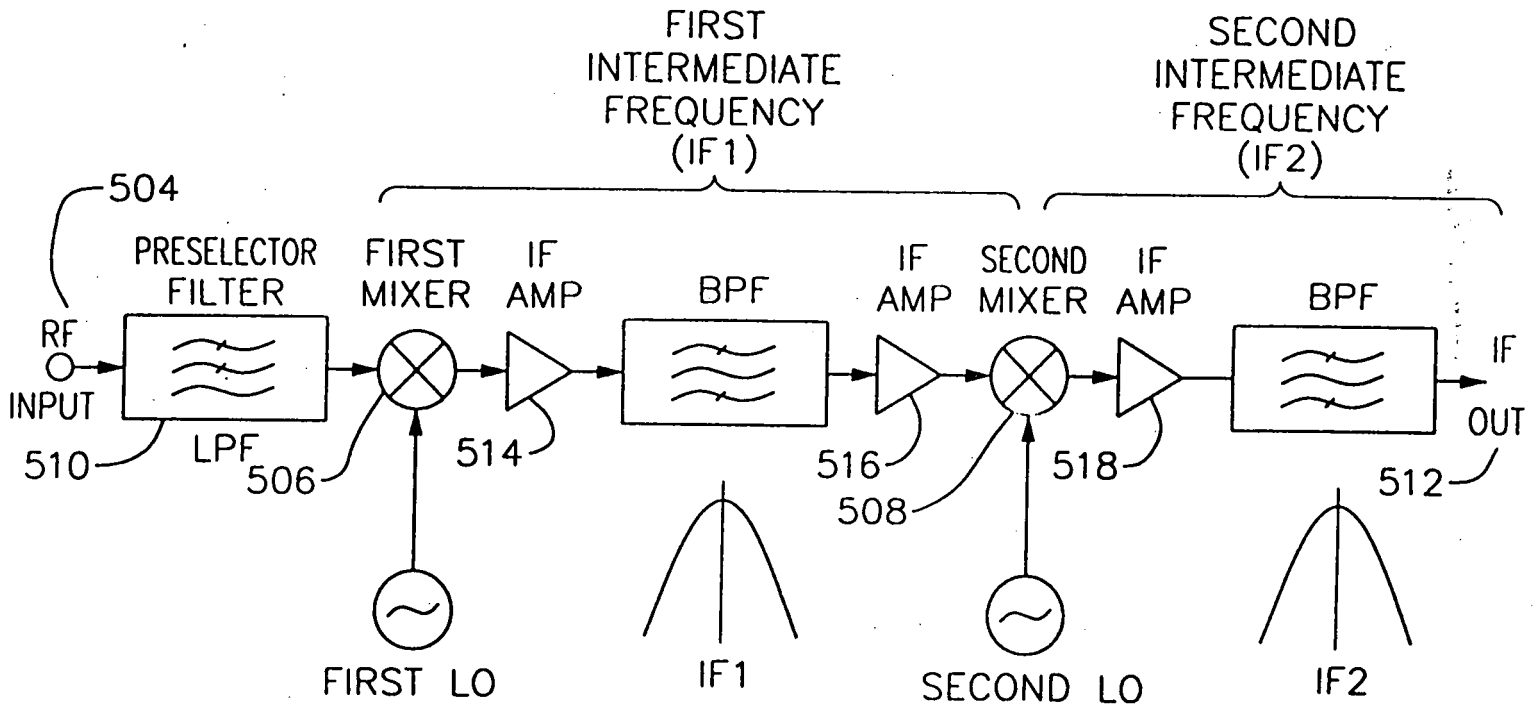
FIG. 4
PRIOR ART



0082F0" 2h626h60

FIG.5

DUAL CONVERSION RECEIVER



IF2<RFINPUT<IF1

FIG. 6

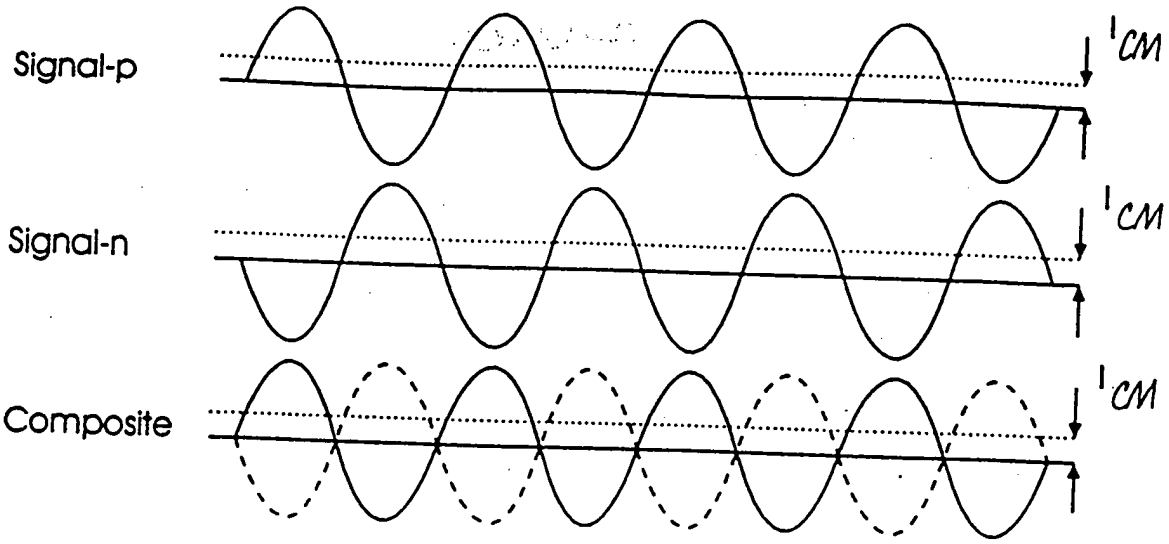

Signal-p
Signal-n
Composite
1 CM
1 CM
1 CM

FIG. 7

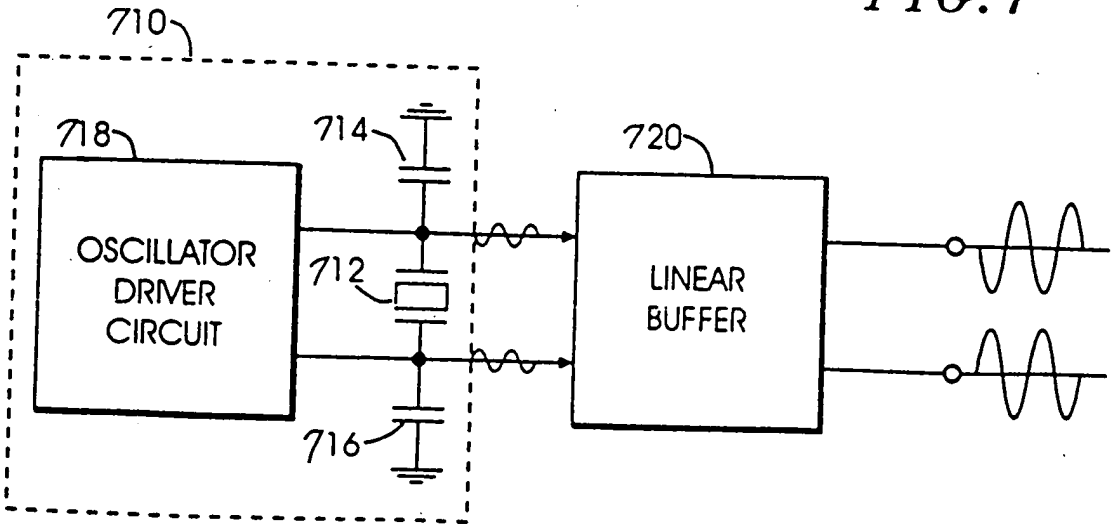

710
718
714
720
OSCILLATOR DRIVER CIRCUIT
712
LINEAR BUFFER
716

FIG. 8

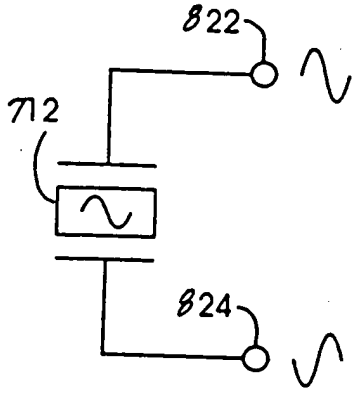


FIG. 9

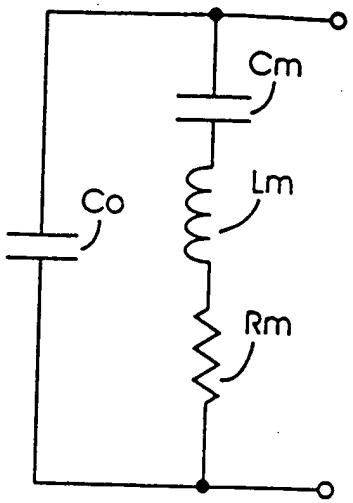


FIG. 10

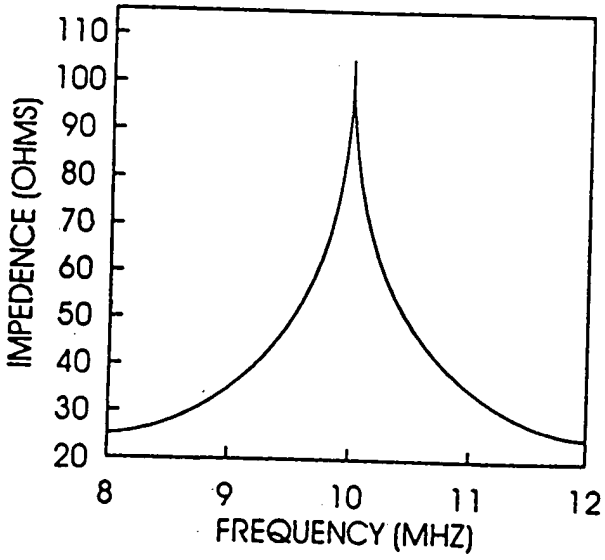


FIG. 11

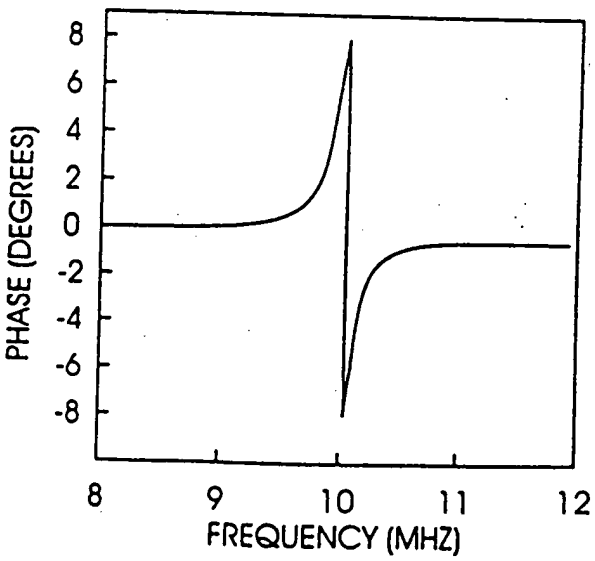


FIG. 12

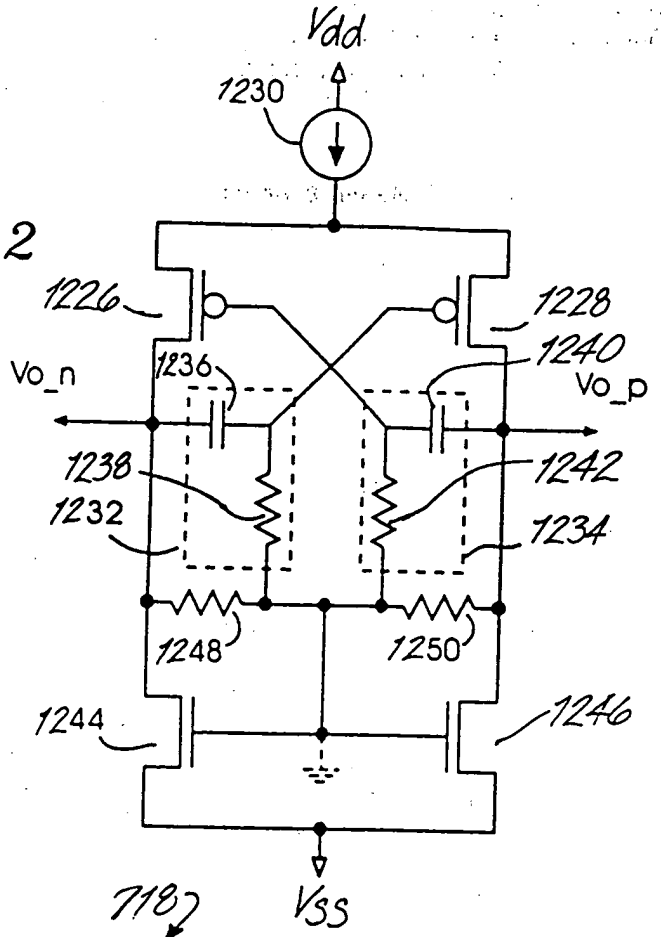

Vdd
1230
1226
1228
1240
Vo_n
1236
Vo_p
1238
1242
1232
1234
1248
1250
1244
1246
Vss

FIG. 13

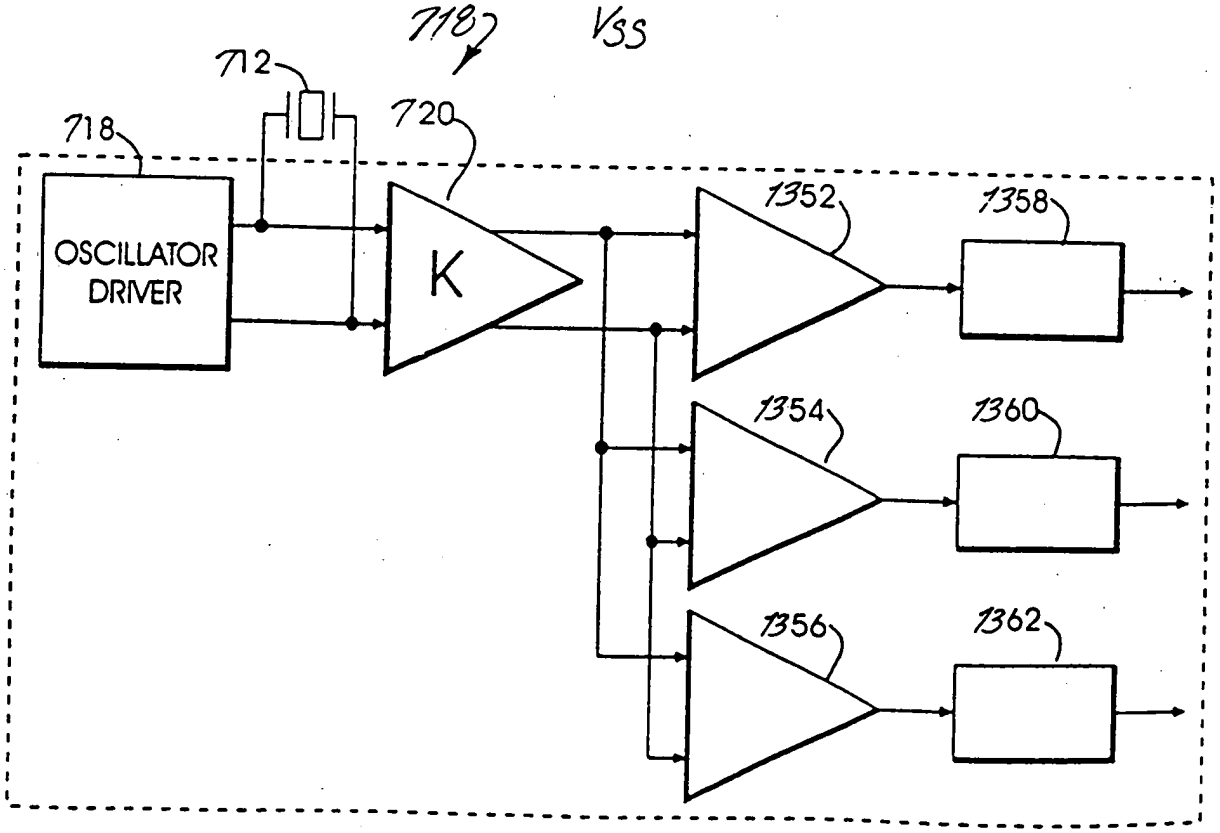
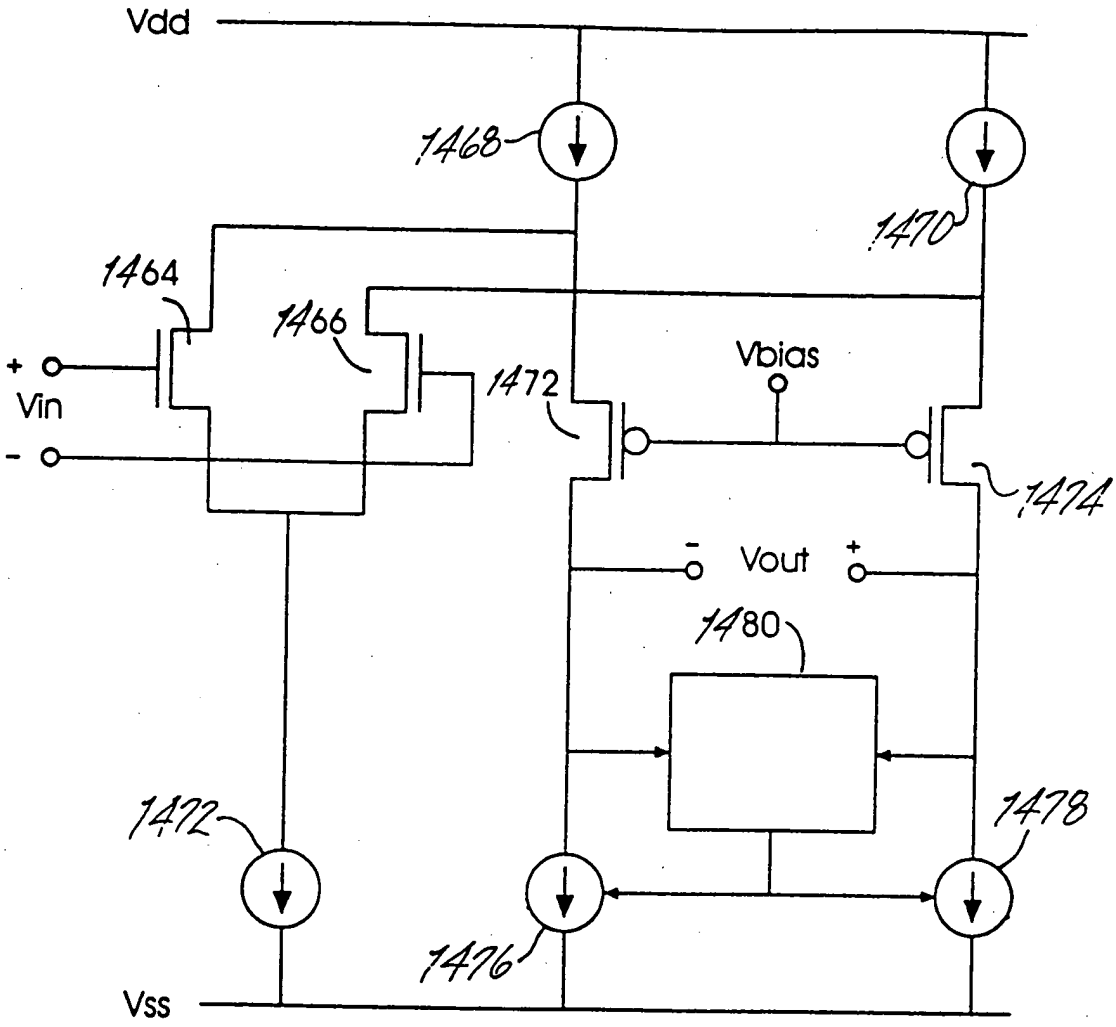

718
712
720
718
OSCILLATOR DRIVER
K
1352
1358
1354
1360
1356
1362

FIG. 14


Vdd
1468
1470
1464
1466
+
Vin
-
1472
Vbias
1474
-
Vout
+
1480
1472
1478
1476
Vss

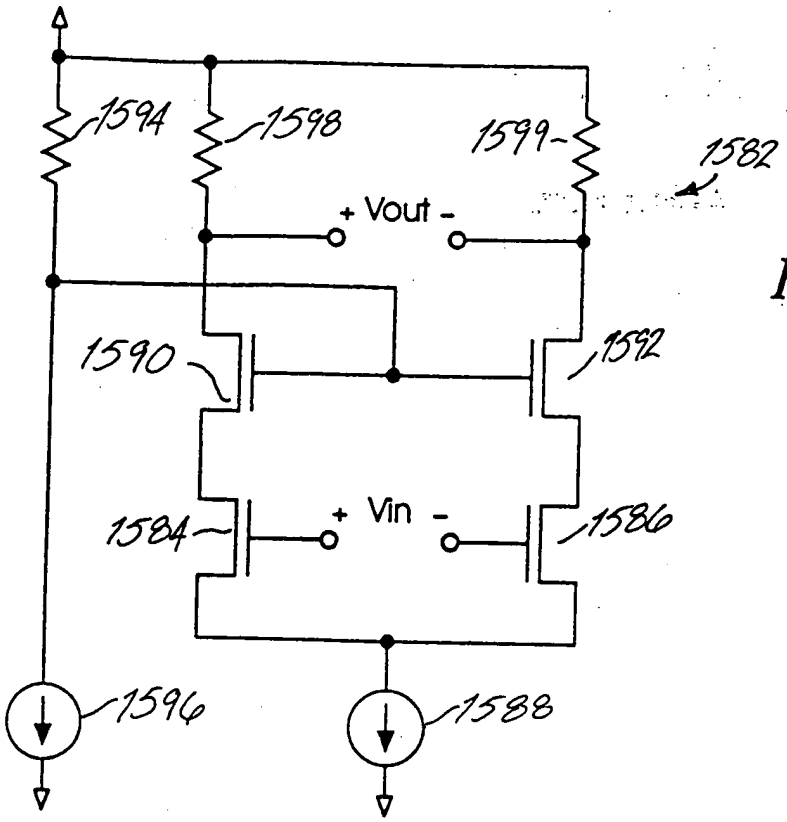

1594
1598
1599
1582
+ Vout -
1590
1592
1584
+ Vin -
1586
1596
1588

FIG. 15

FIG. 16

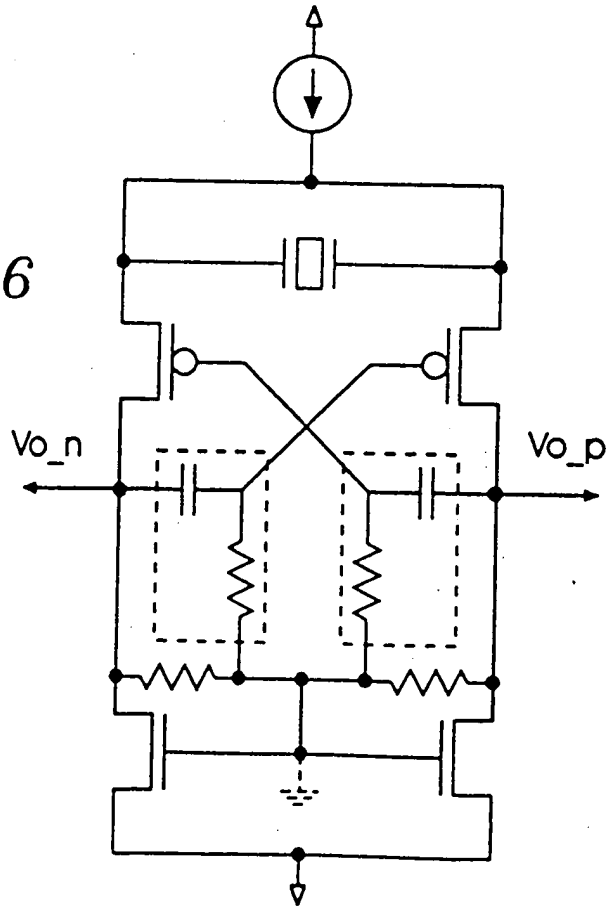

Vo_n
Vo_p

FIG. 17

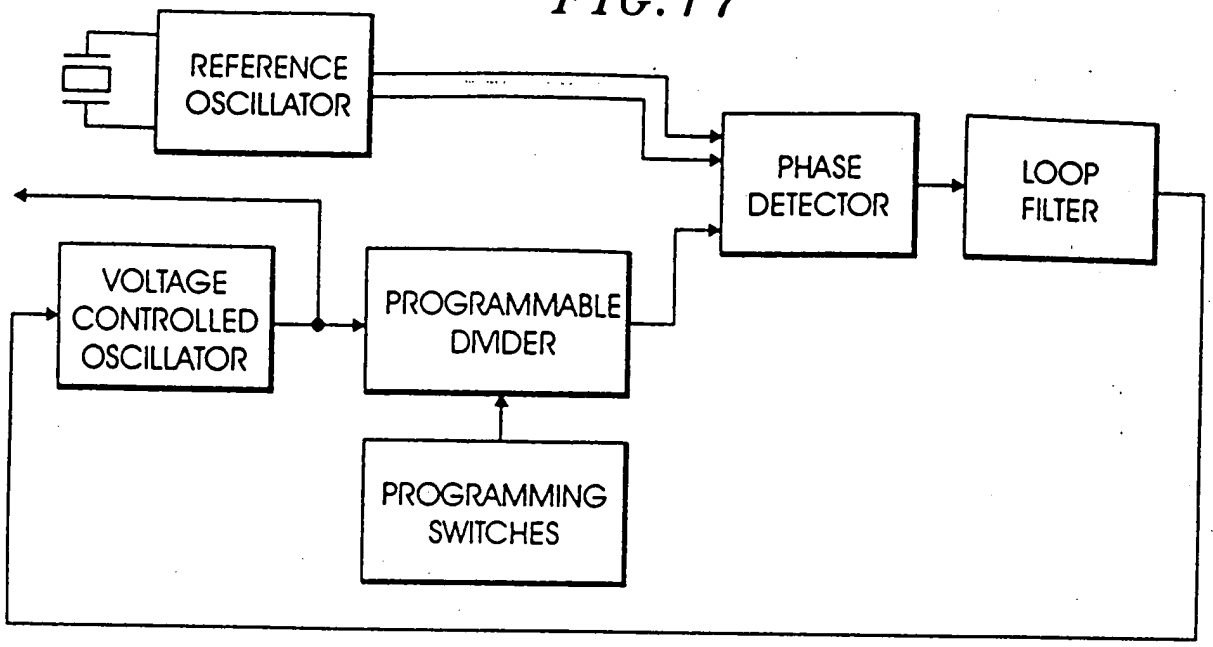
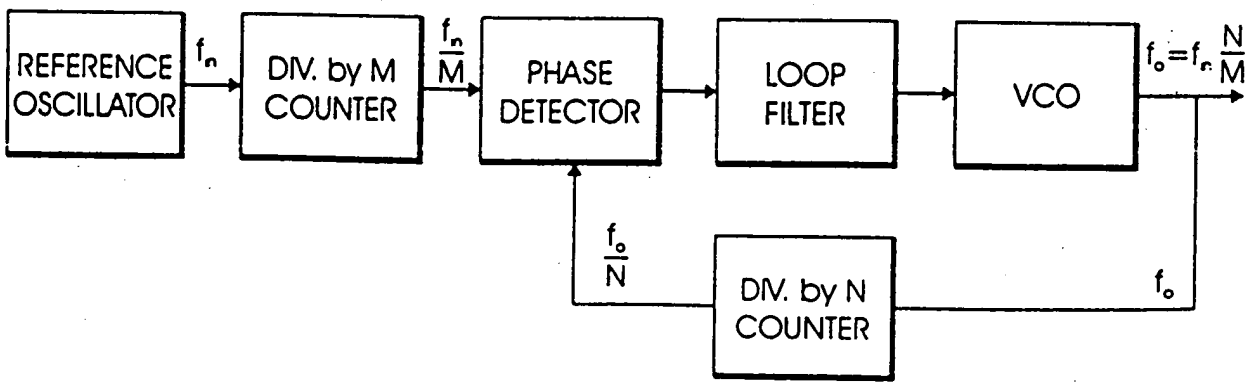
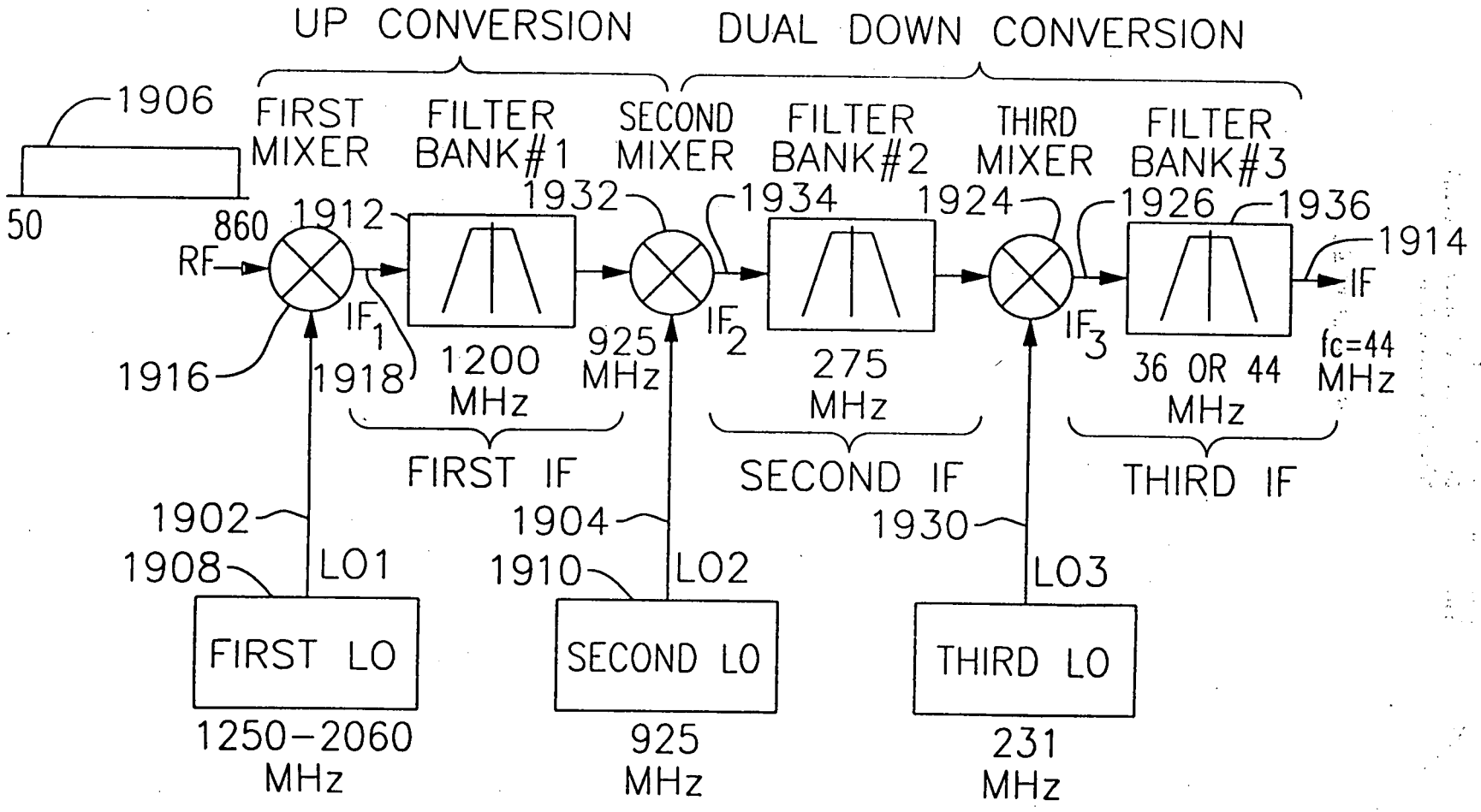

REFERENCE OSCILLATOR
PHASE DETECTOR
LOOP FILTER
VOLTAGE CONTROLLED OSCILLATOR
PROGRAMMABLE DIVIDER
PROGRAMMING SWITCHES

FIG. 18


REFERENCE OSCILLATOR
f_n
DIV. by M COUNTER
$\frac{f_n}{M}$
PHASE DETECTOR
LOOP FILTER
VCO
$f_o = f_n \frac{N}{M}$
$\frac{f_o}{N}$
DIV. by N COUNTER
f_o

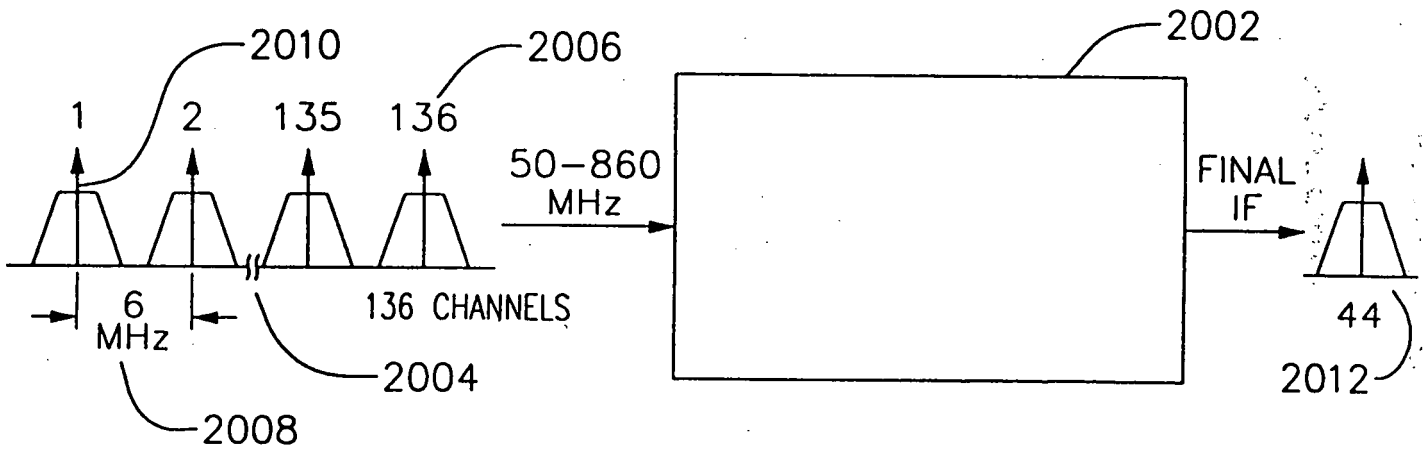
0086TD" 2h6E6h60

FIG. 19



6,052,160

FIG.20



0082702 2A6A60

FIG.21

PPL Xtal REFERENCE=10MHz
LO-1, 10MHz FREQUENCY STEPS
LO-2, 100kHz FREQUENCY STEPS

44MHz IF

TABLE OF FREQUENCIES BASED ON COARSE/FINE PLL SOLUTION:

NOTE
- LO-2 REF=100KHz, SO DIVIDE RANGE=9216 TO 9280

Frf (MHz)	50	56	62	68	74	80	86	92	98	104	110	116	122	128	"	854	860
LO-1(MHz)	1250	1260	1260	1270	1270	1280	1290	1290	1300	1300	1310	1320	1320	1330	"	2050	2060
IF-1 (MHz)	**1200**	1204	1198	1202	1196	**1200**	1204	1198	1202	1196	**1200**	1204	1198	1202	"	1196	**1200**
LO-2(MHz)	**924.8**	928.0	923.2	926.4	921.6	**924.8**	928.0	923.2	926.4	921.6	**924.8**	928.0	923.2	926.4	"	921.6	**924.8**
IF-2(MHz)	275.2	276.0	274.8	275.6	274.4	**275.2**	276.0	274.8	275.6	274.4	**275.2**	276.0	274.8	275.6	"	274.4	**275.2**
LO-3(MHz)	231.2	232	230.8	232	230	231	232	231	232	230	231	232	231	232	"	230	231
IF-3(MHz)	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	"	44.0	44.0

2102

0820 2626

FIG.22

PPL Xtal REFERENCE=10MHz
LO-1, 10MHz FREQUENCY STEPS
LO-2, 100kHz FREQUENCY STEPS

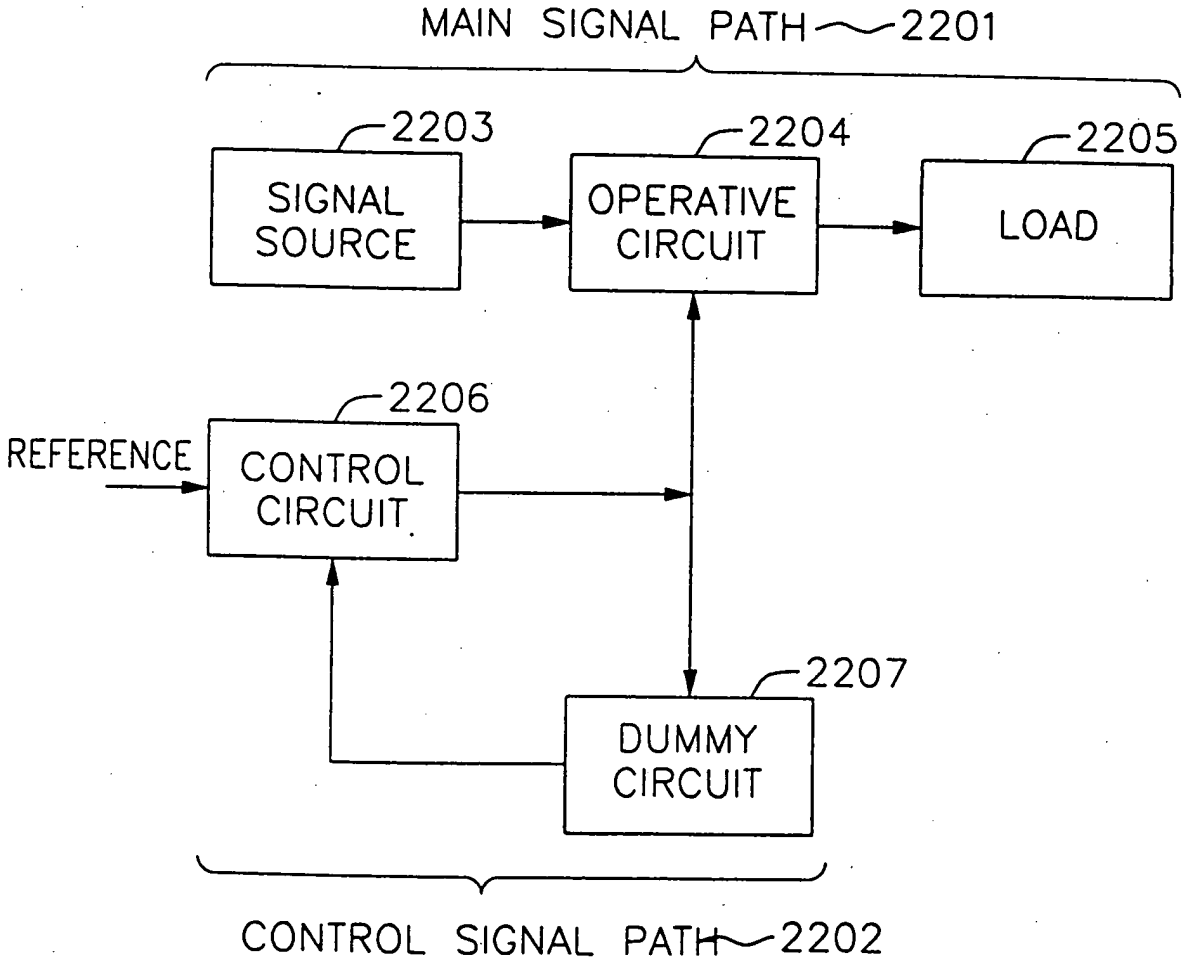
36MHz IF

TABLE OF FREQUENCIES BASED ON COARSE/FINE PLL SOLUTION:

NOTE
- LO-2 REF=100KHz, SO DIVIDE RANGE=9280 TO 9340

Frf (MHz)	50	58	66	74	82	90	98	106	114	122	130	138	146	154	"	852	860
LO-1(MHz)	1250	1260	1270	1270	1280	1290	1300	1310	1310	1320	1330	1340	1350	1350	"	2050	2060
IF-1 (MHz)	1200	1202	1204	1196	1198	1200	1202	1204	1196	1198	1200	1202	1204	1196	"	1198	1200
LO-2(MHz)	931.2	932.8	934.4	928.0	930	931	933	934	928.0	930	931	933	934	928.0	"	929.60	931.2
IF-2(MHz)	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	"	268.4	268.8
LO-3(MHz)	232.8	233.2	233.6	232	232	233	233	234	232	232	233	233	234	232.0	"	232.4	232.8
IF-3(MHz)	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	"	36.0	36.0

FIG.23


MAIN SIGNAL PATH
2201
2203
SIGNAL SOURCE
2204
OPERATIVE CIRCUIT
2205
LOAD
2206
REFERENCE
CONTROL CIRCUIT
2207
DUMMY CIRCUIT
CONTROL SIGNAL PATH
2202

08270 "26260

FIG.24a

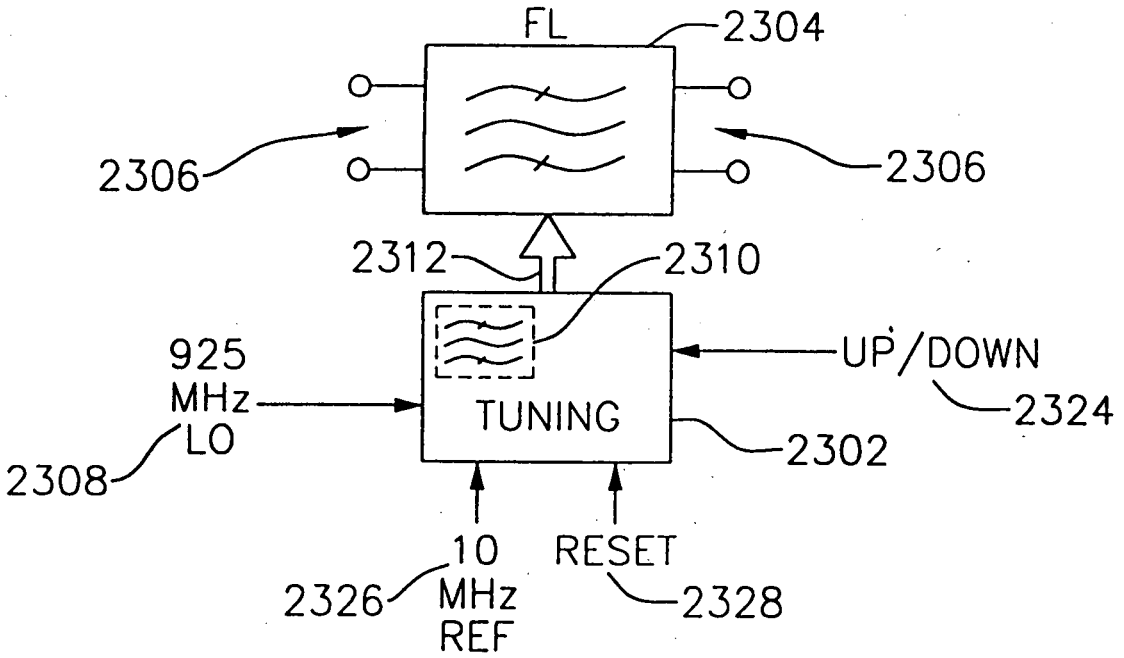
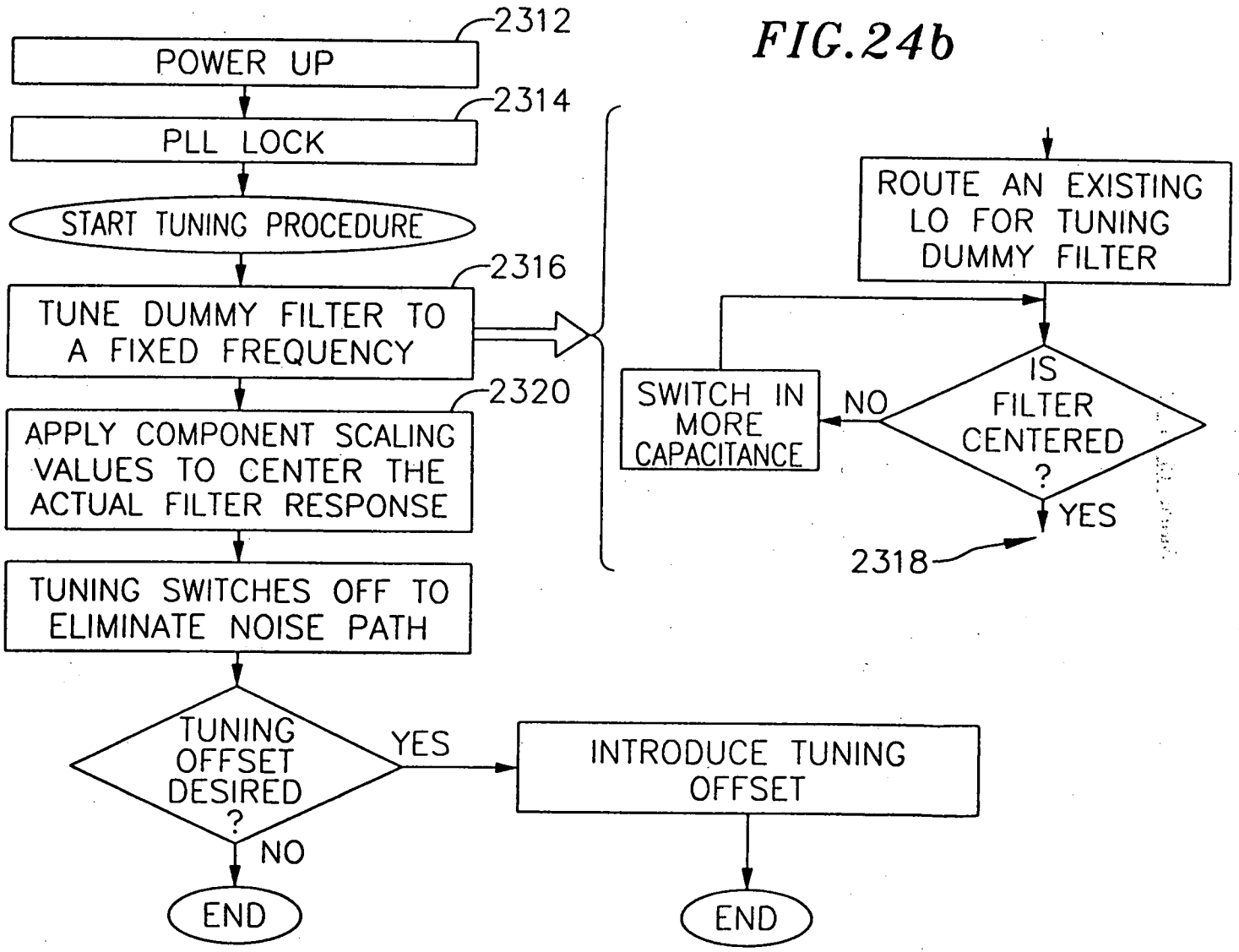
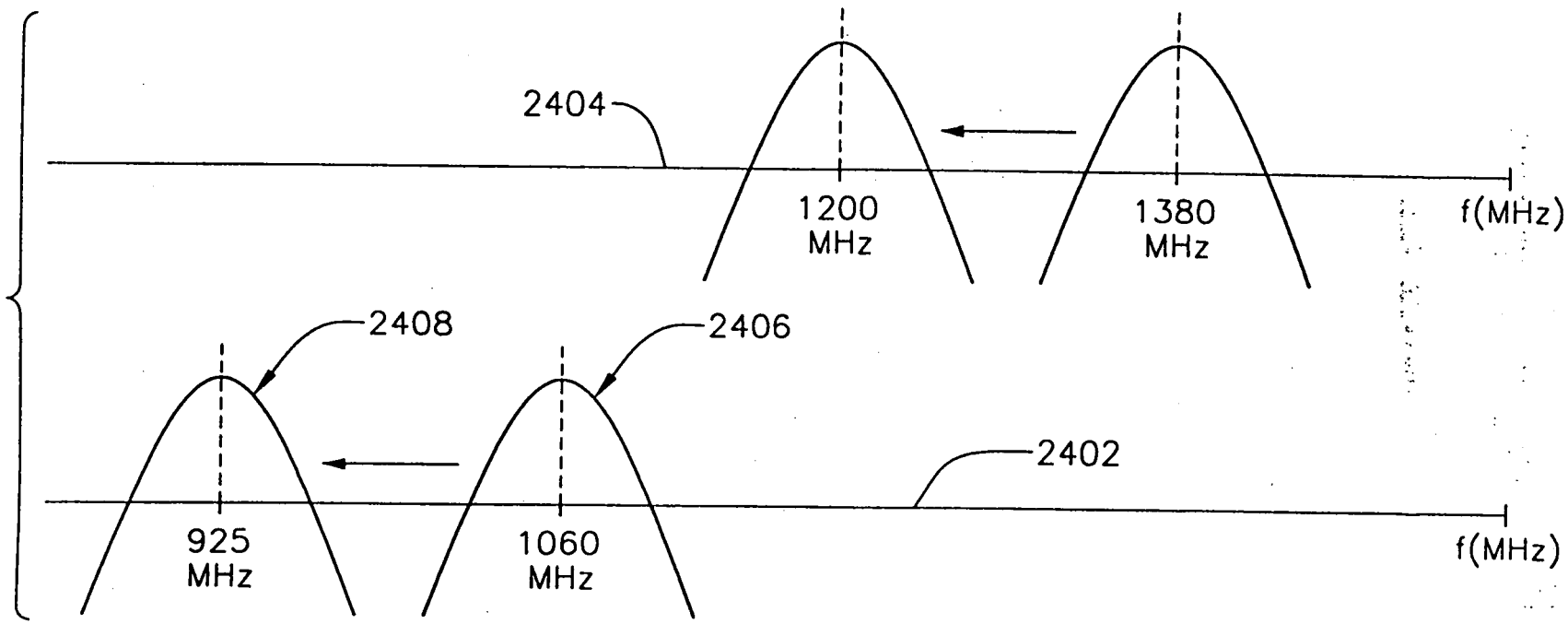


FIG.24b


2312
POWER UP
2314
PLL LOCK
START TUNING PROCEDURE
2316
TUNE DUMMY FILTER TO A FIXED FREQUENCY
2320
APPLY COMPONENT SCALING VALUES TO CENTER THE ACTUAL FILTER RESPONSE
TUNING SWITCHES OFF TO ELIMINATE NOISE PATH
TUNING OFFSET DESIRED ?
YES
NO
END
INTRODUCE TUNING OFFSET
END
ROUTE AN EXISTING LO FOR TUNING DUMMY FILTER
IS FILTER CENTERED ?
NO
SWITCH IN MORE CAPACITANCE
YES
2318

08870 "26626

FIG.24c



Doc ID: EP 0 884 848 A2

FIG.25

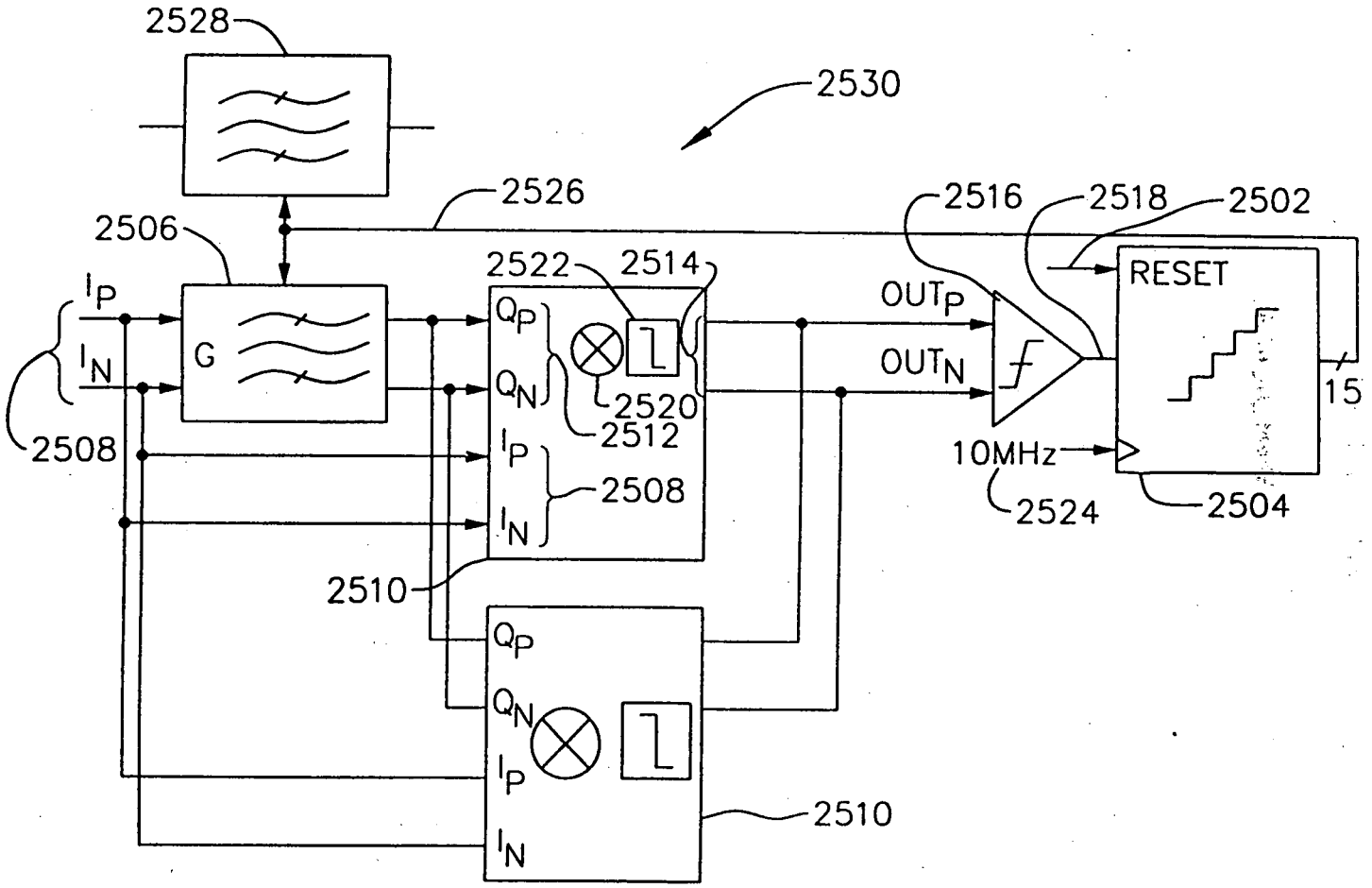


FIG.26

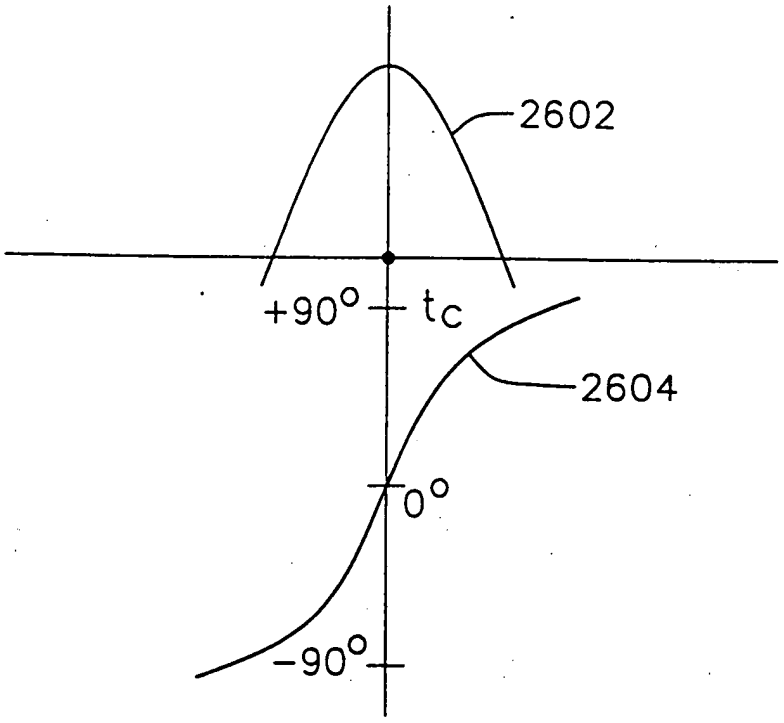


FIG.27

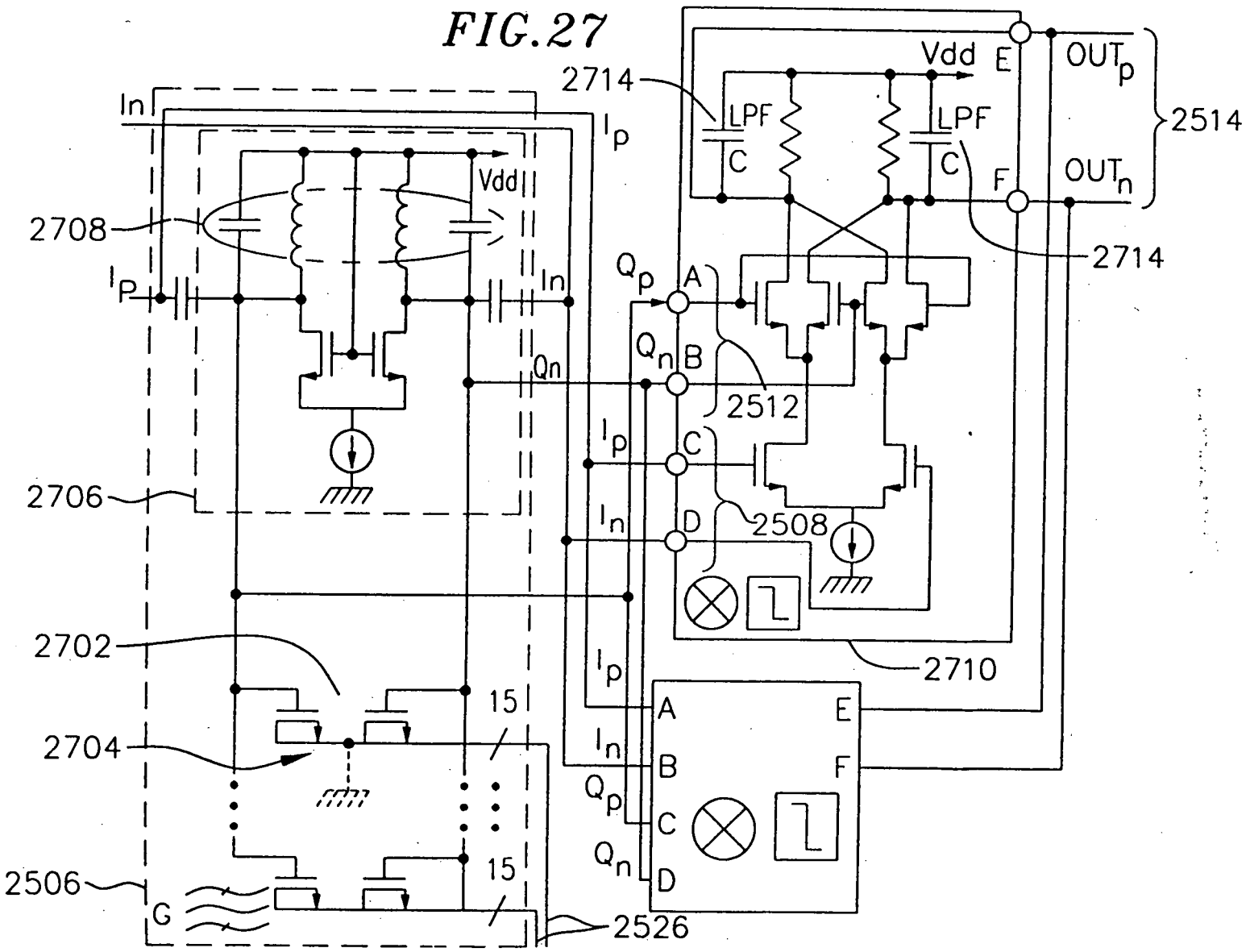
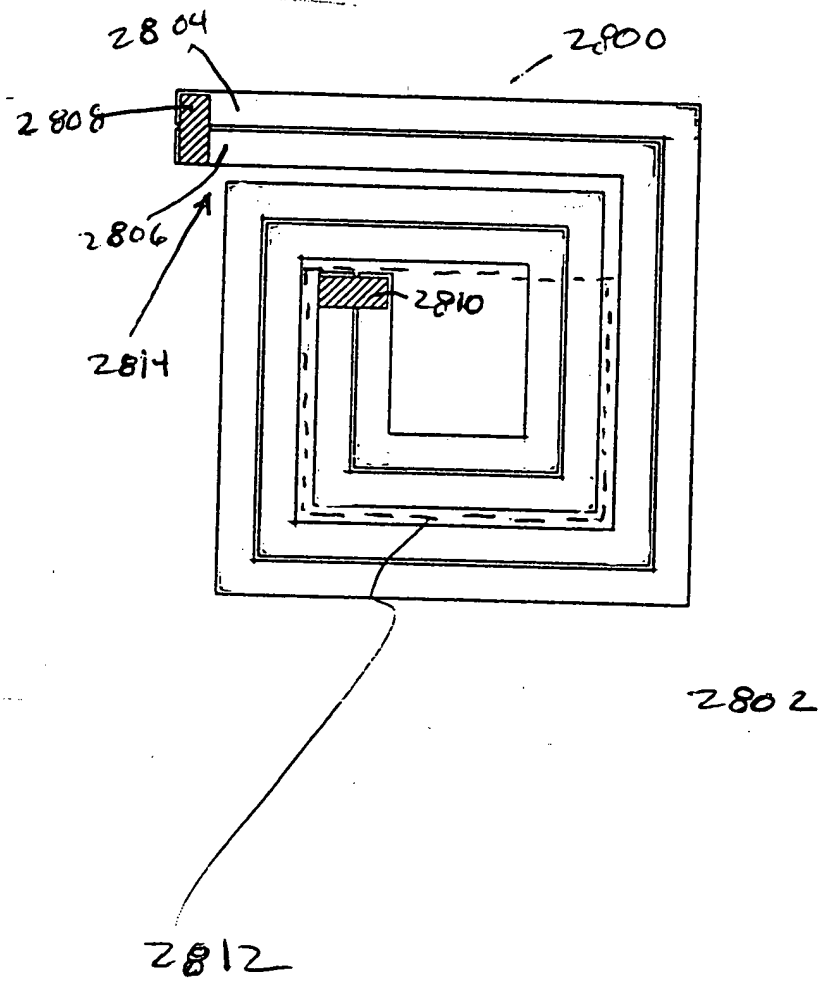

In
I_p
Vdd
2708
I_p
In
Qn
2706
2702
2704
2506
G
15
15
2526
2714
LPF
C
Vdd
E
OUT_p
2514
F
OUT_n
2714
Q_p
A
Q_n
B
2512
I_p
C
I_n
D
2508
2710
I_p
A
I_n
B
Q_p
C
Q_n
D
E
F

FIG.28a



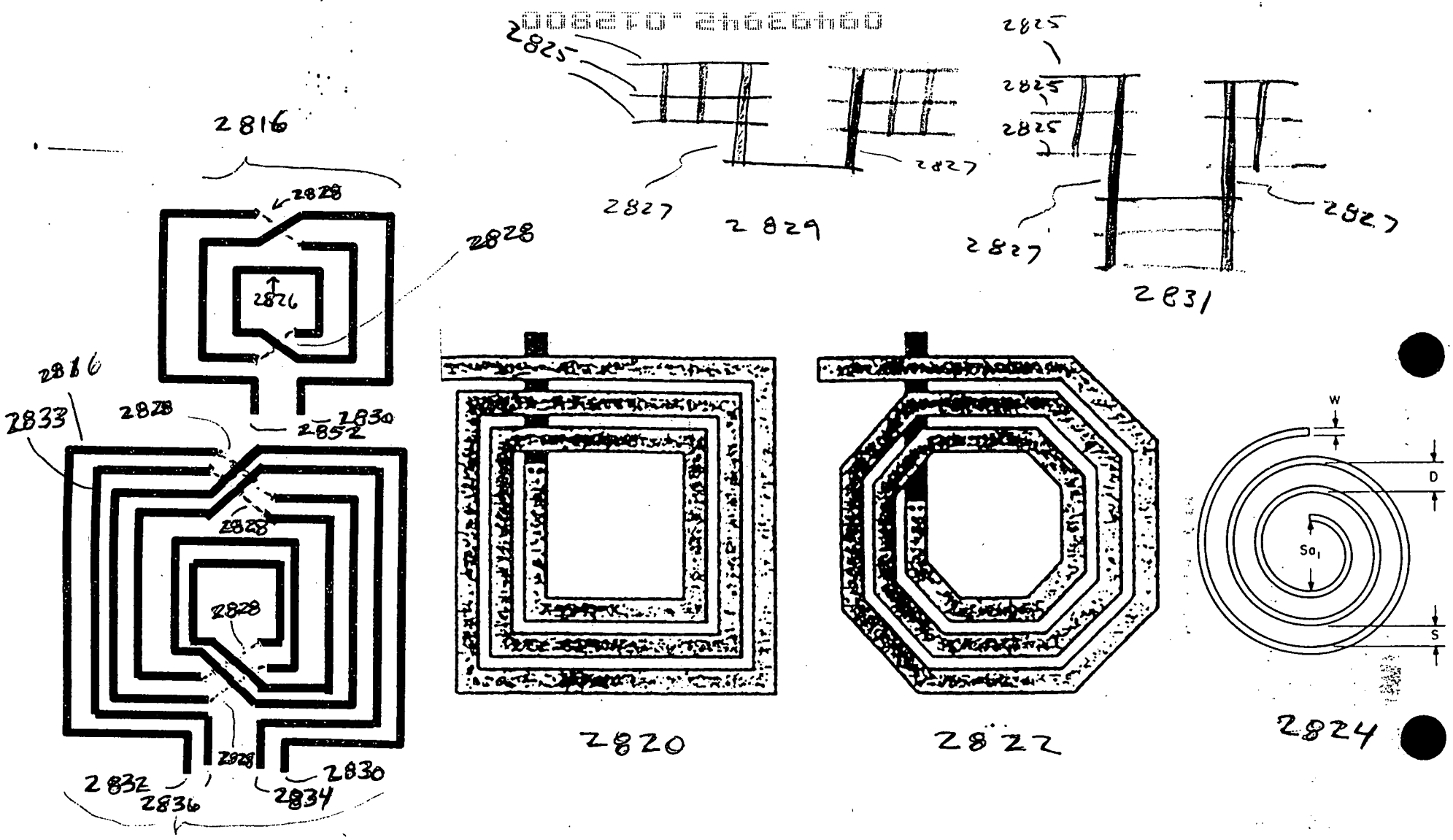

2816
2828
2826
2828
2816
2833
2828
2830
2852
2828
2828
2832
2836
2828
2834
2830
2818
2825
2827
2829
2825
2825
2825
2827
2827
2831
2820
2822
W
D
S
2824

FIG 28b

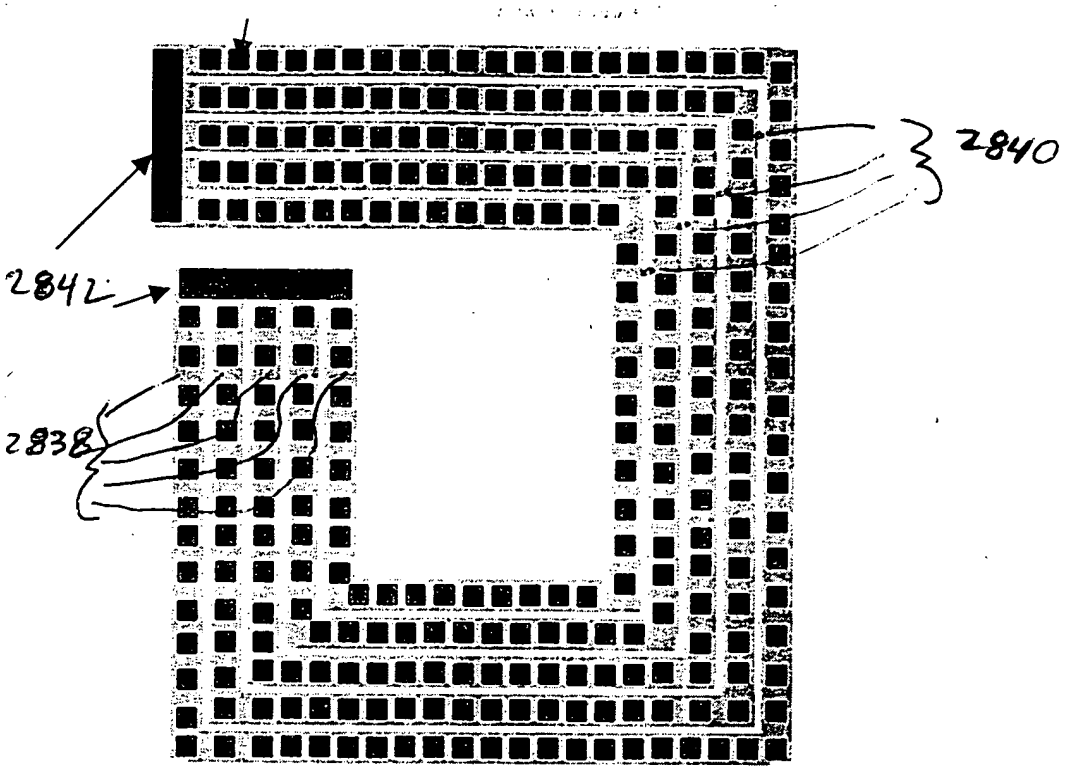


FIG 28c

08210 2h62ch60

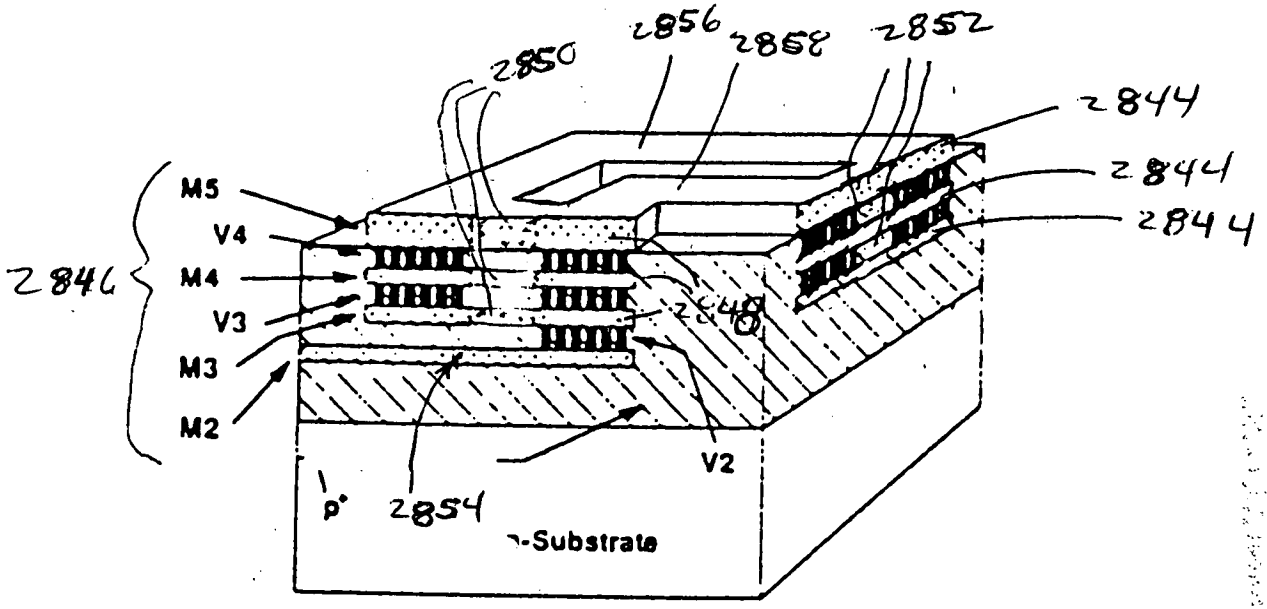


FIG 28d

DOCKET ARCHIVE

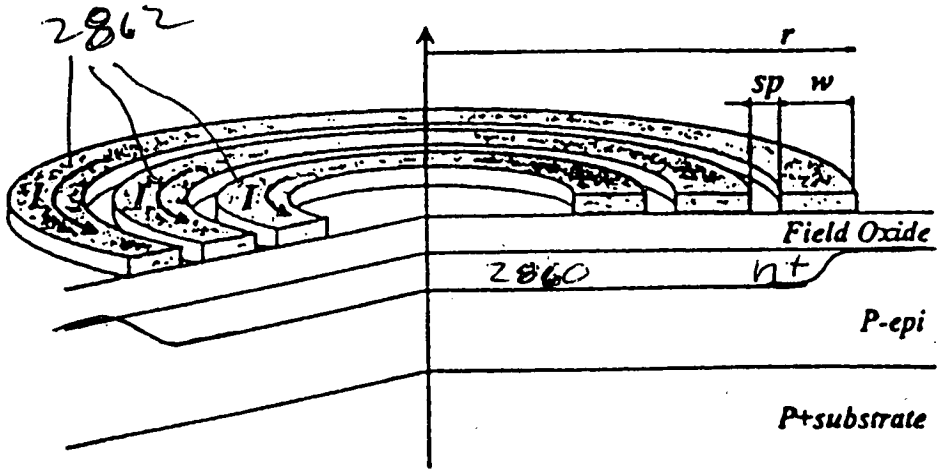


FIG 28e

08270 2862

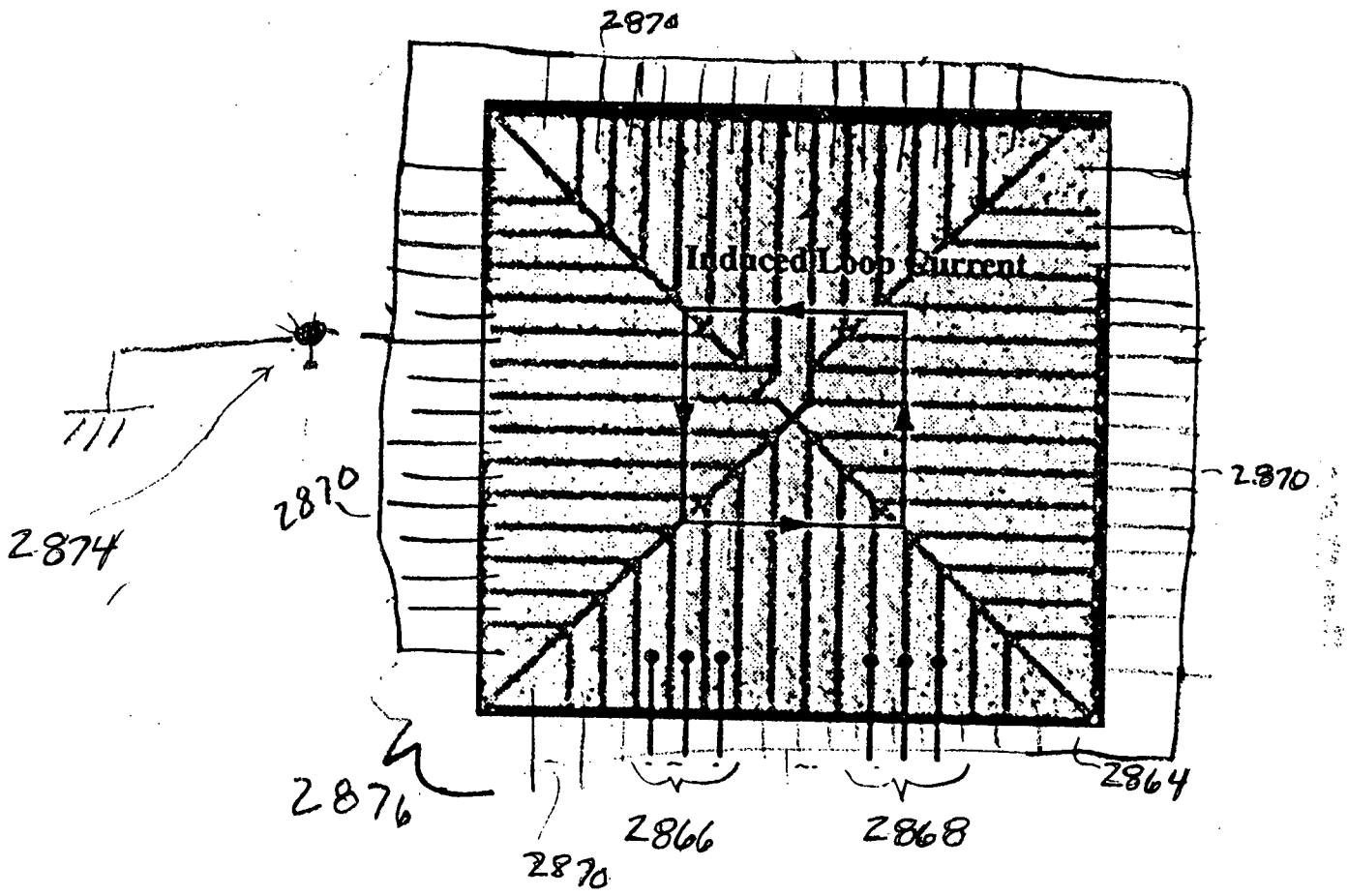


FIG 28 f

FIG.29

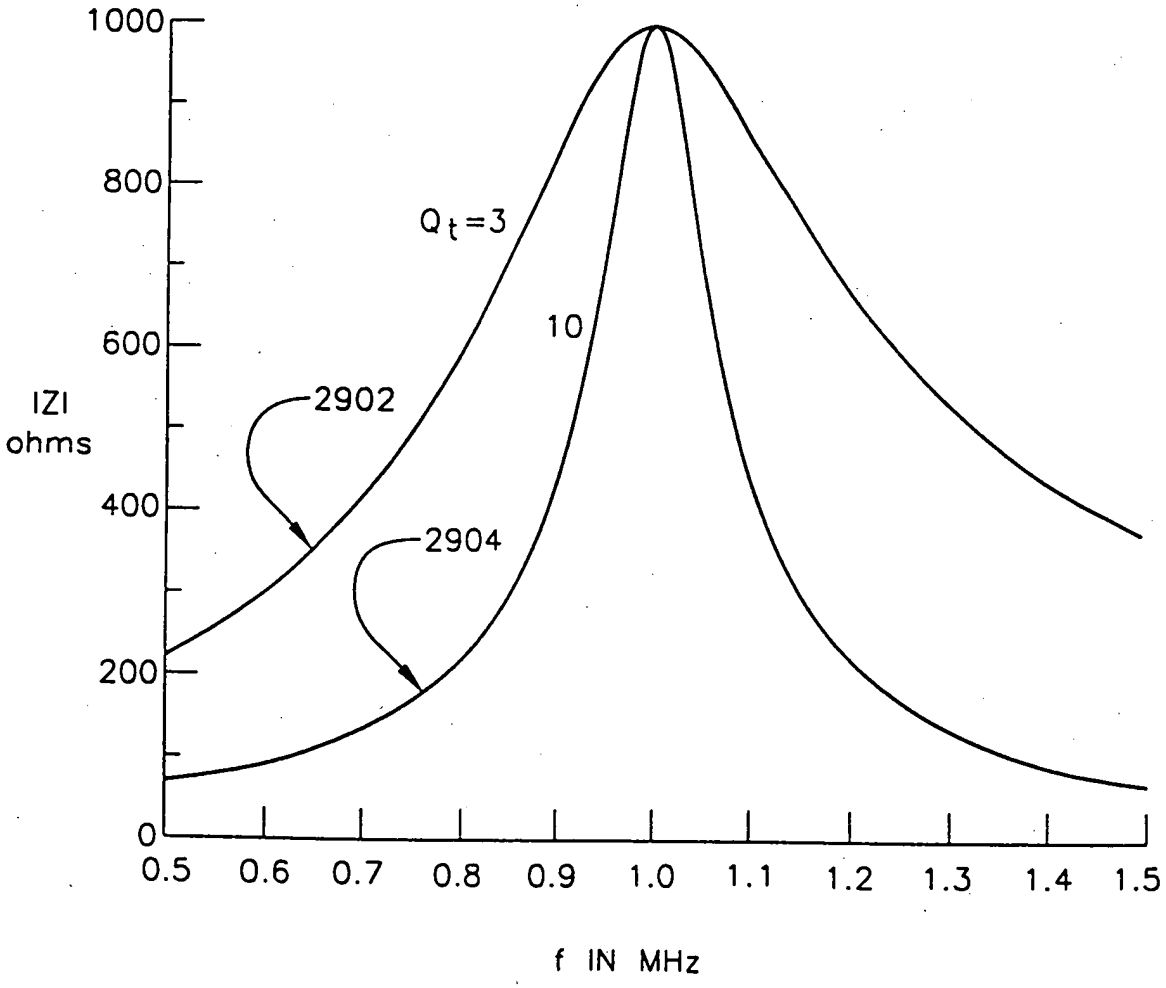

1000
800
600
400
200
0
IZI
ohms
Q_t=3
10
2902
2904
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
1.3
1.4
1.5
f IN MHz

FIG.30

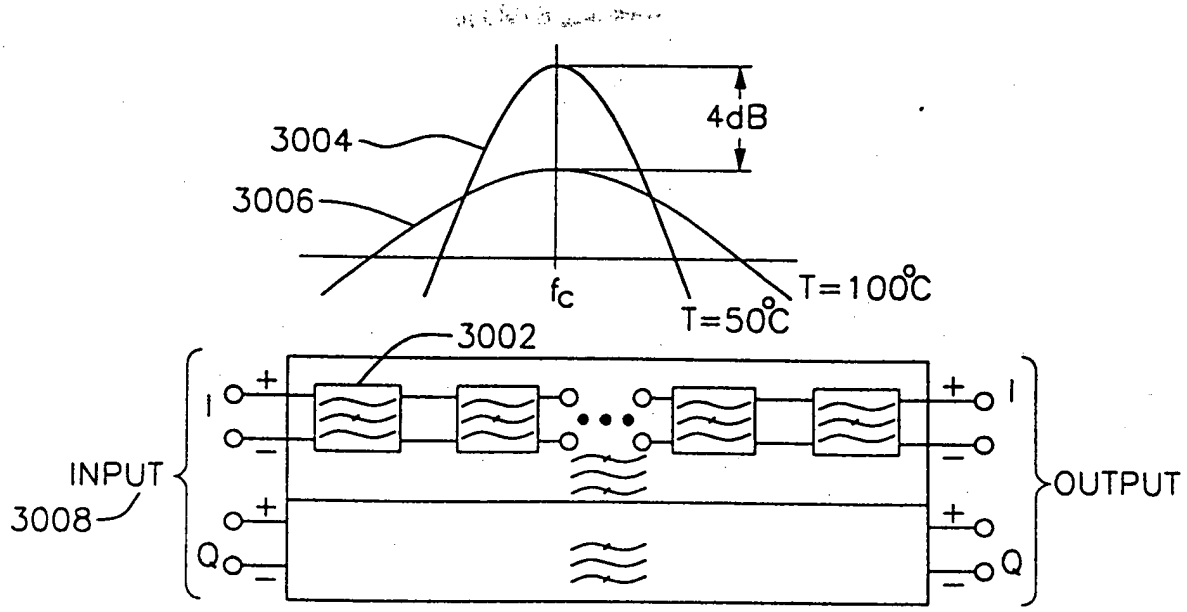
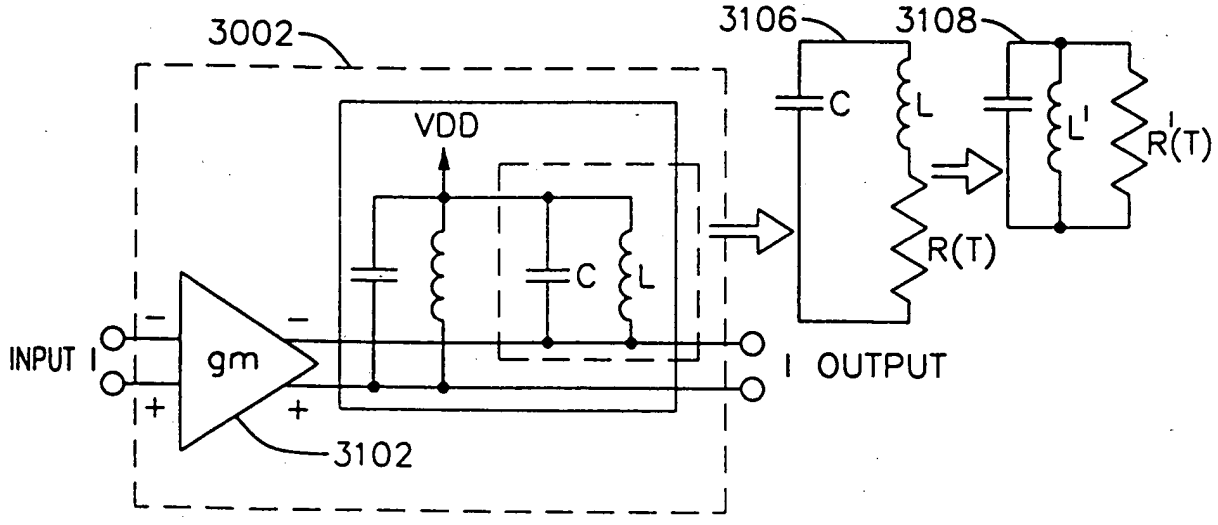
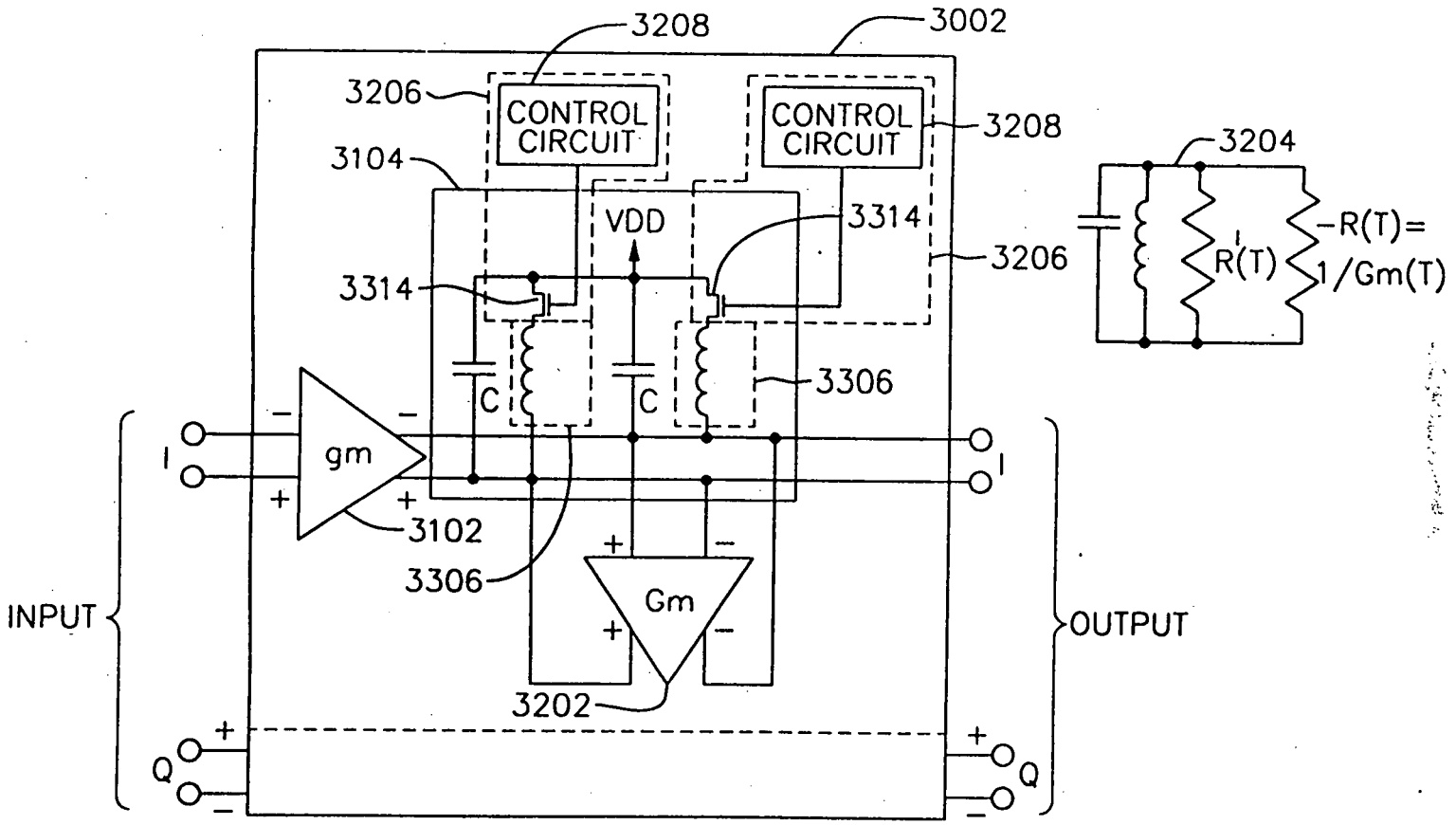

4dB
3004
3006
f_c
T=100°C
T=50°C
3002
INPUT
3008
I
Q
OUTPUT

FIG.31


3002
3106
3108
VDD
C
L
C
L
R(T)
L'
R'(T)
INPUT I
gm
3102
I OUTPUT

0082T0 2h66h60

FIG.32



0082T0"2h6E6h6D

FIG.33

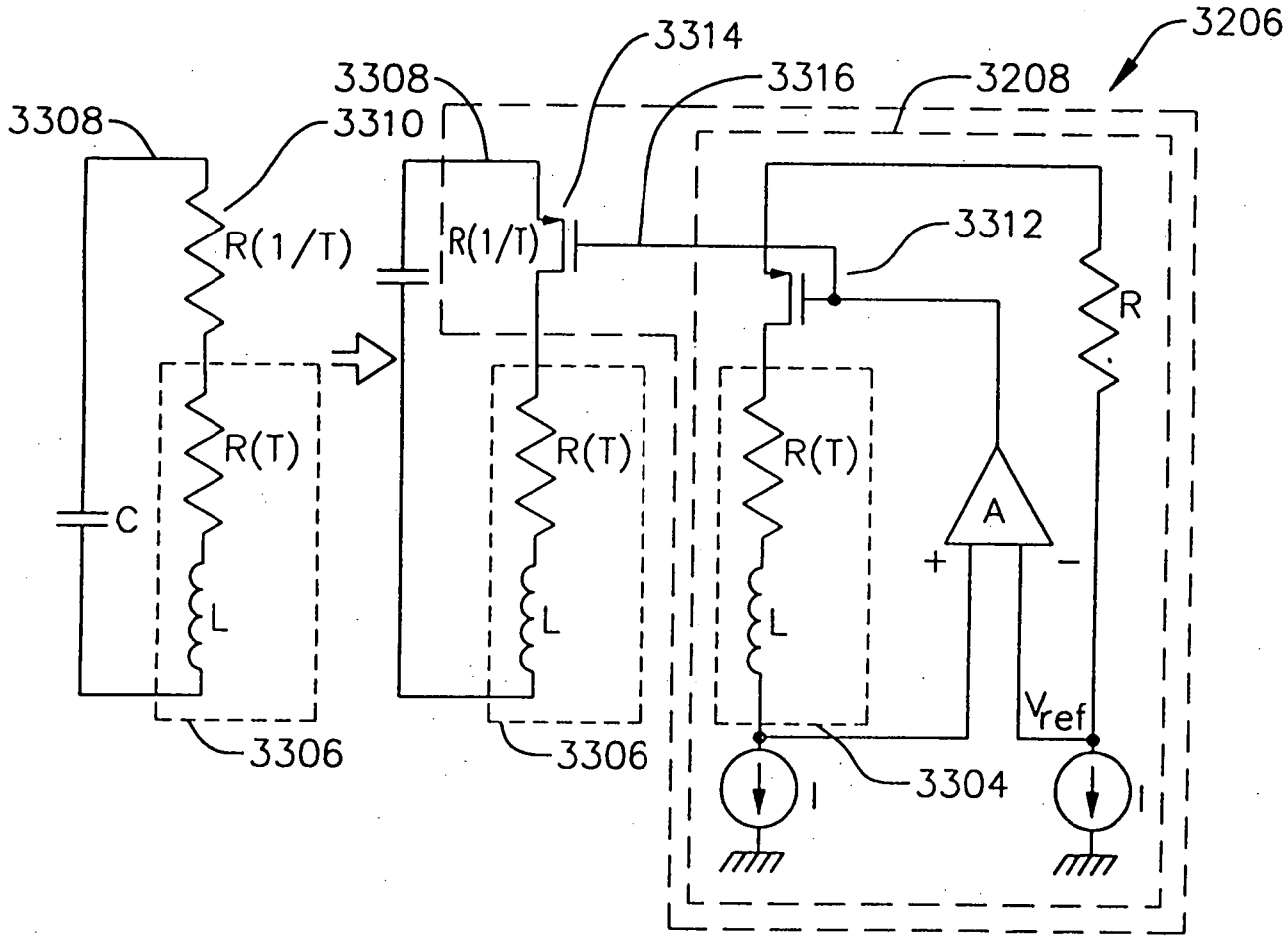


FIG. 34

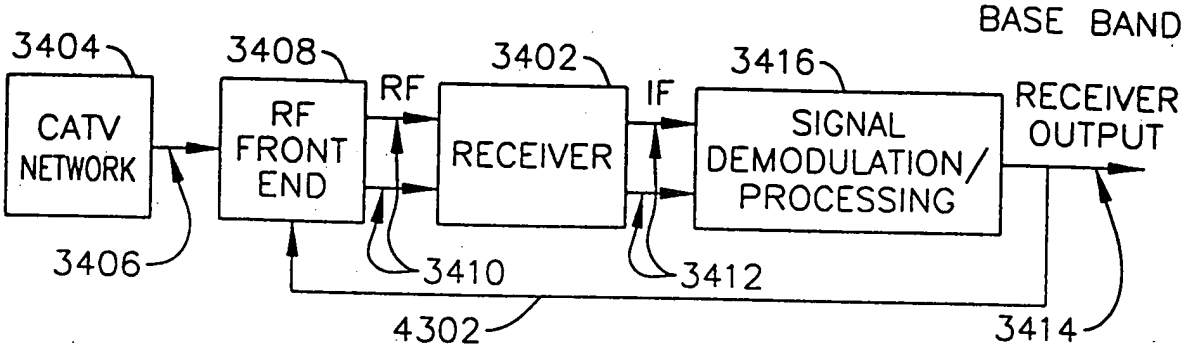
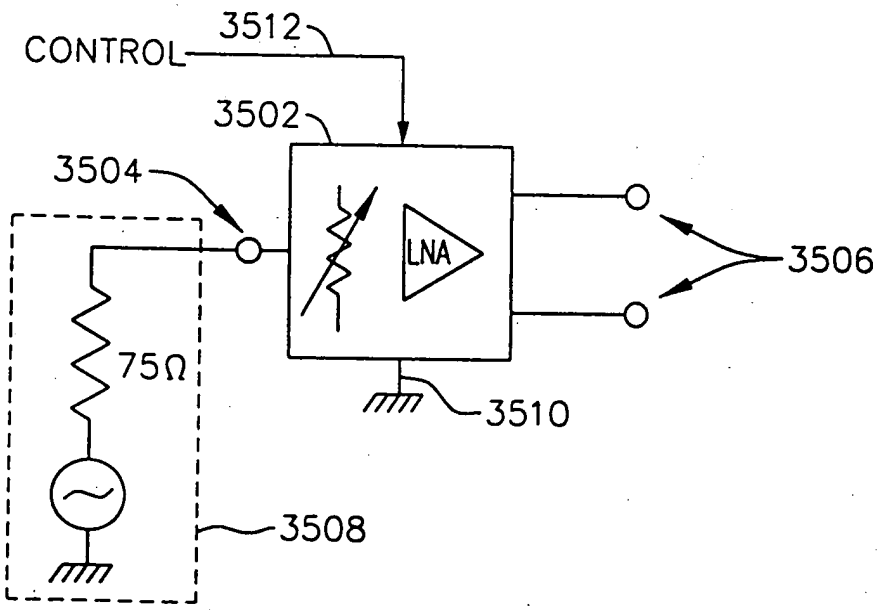
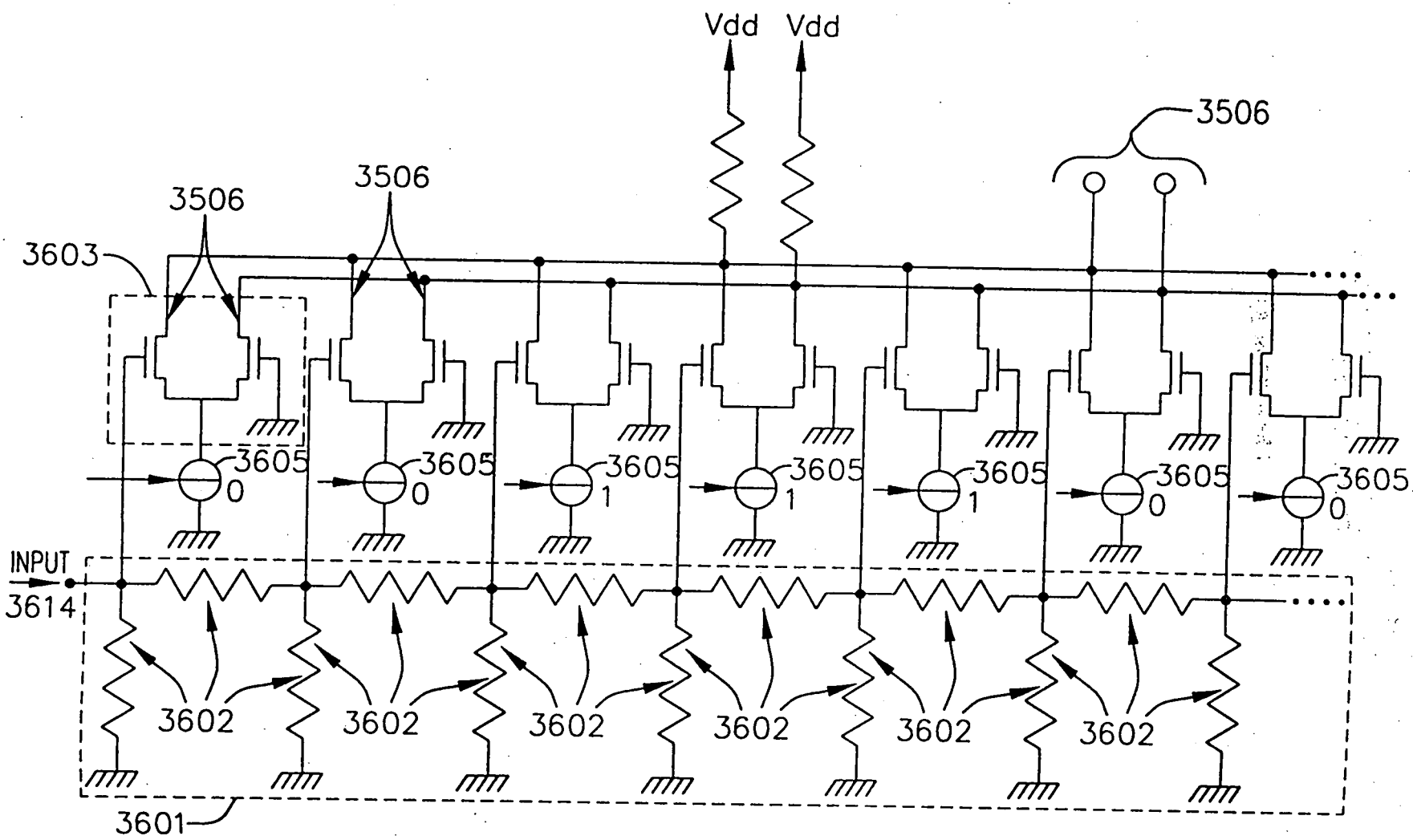

3404
CATV NETWORK
3406
3408
RF FRONT END
RF
3402
RECEIVER
IF
3416
SIGNAL DEMODULATION/ PROCESSING
BASE BAND
RECEIVER OUTPUT
3410
3412
4302
3414

FIG. 35


CONTROL
3512
3502
3504
LNA
3506
75Ω
3510
3508

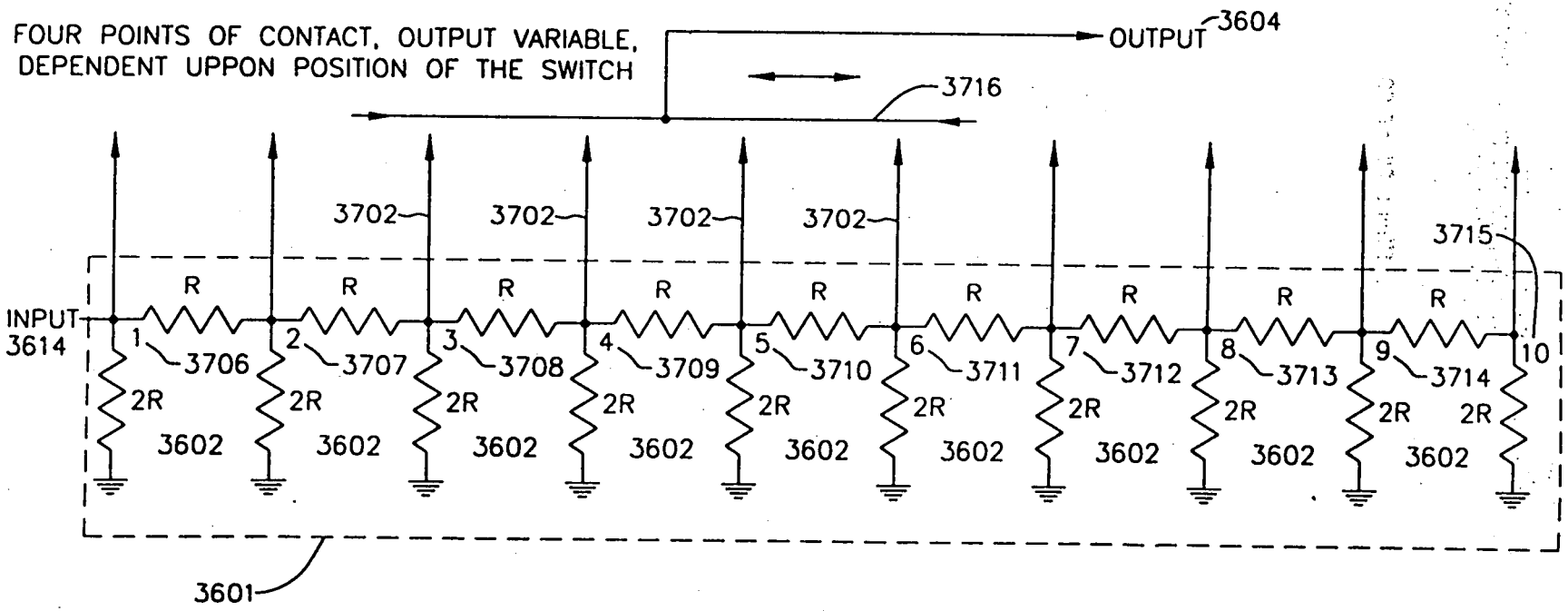
0062T0" 2h6E6h60

FIG.36



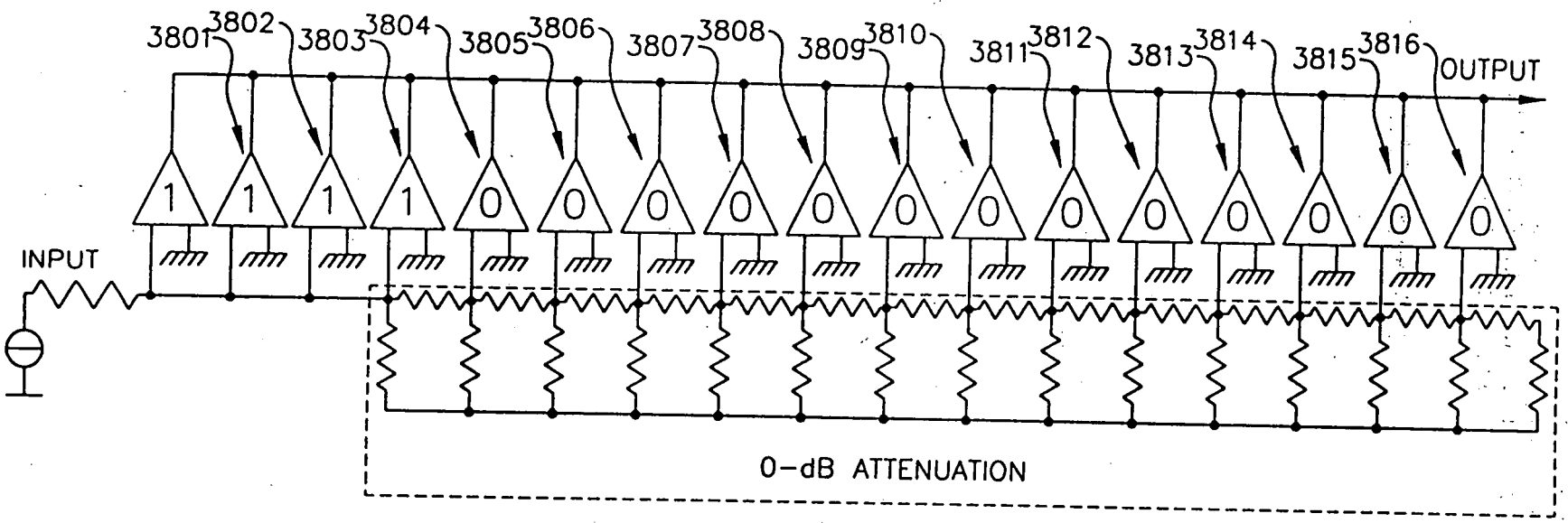
0082T0" 2T62678D

FIG.37



0820"2620h0

FIG.38



08270-260660

FIG.39

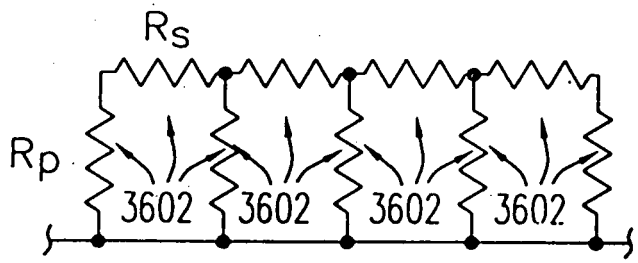
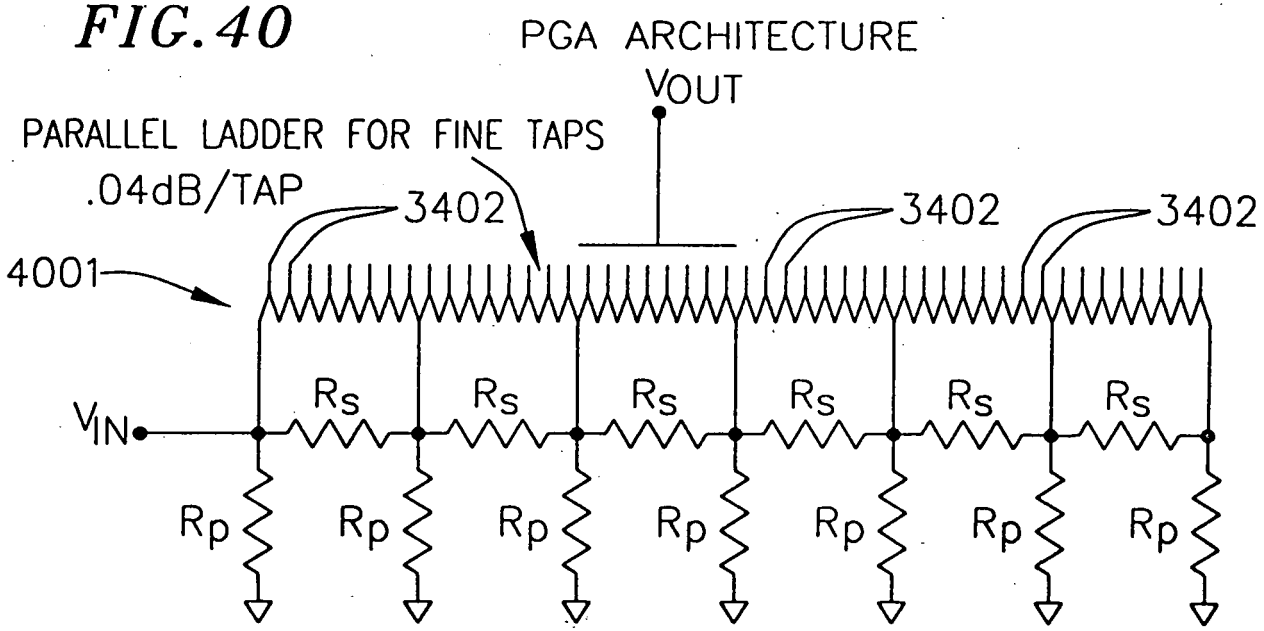
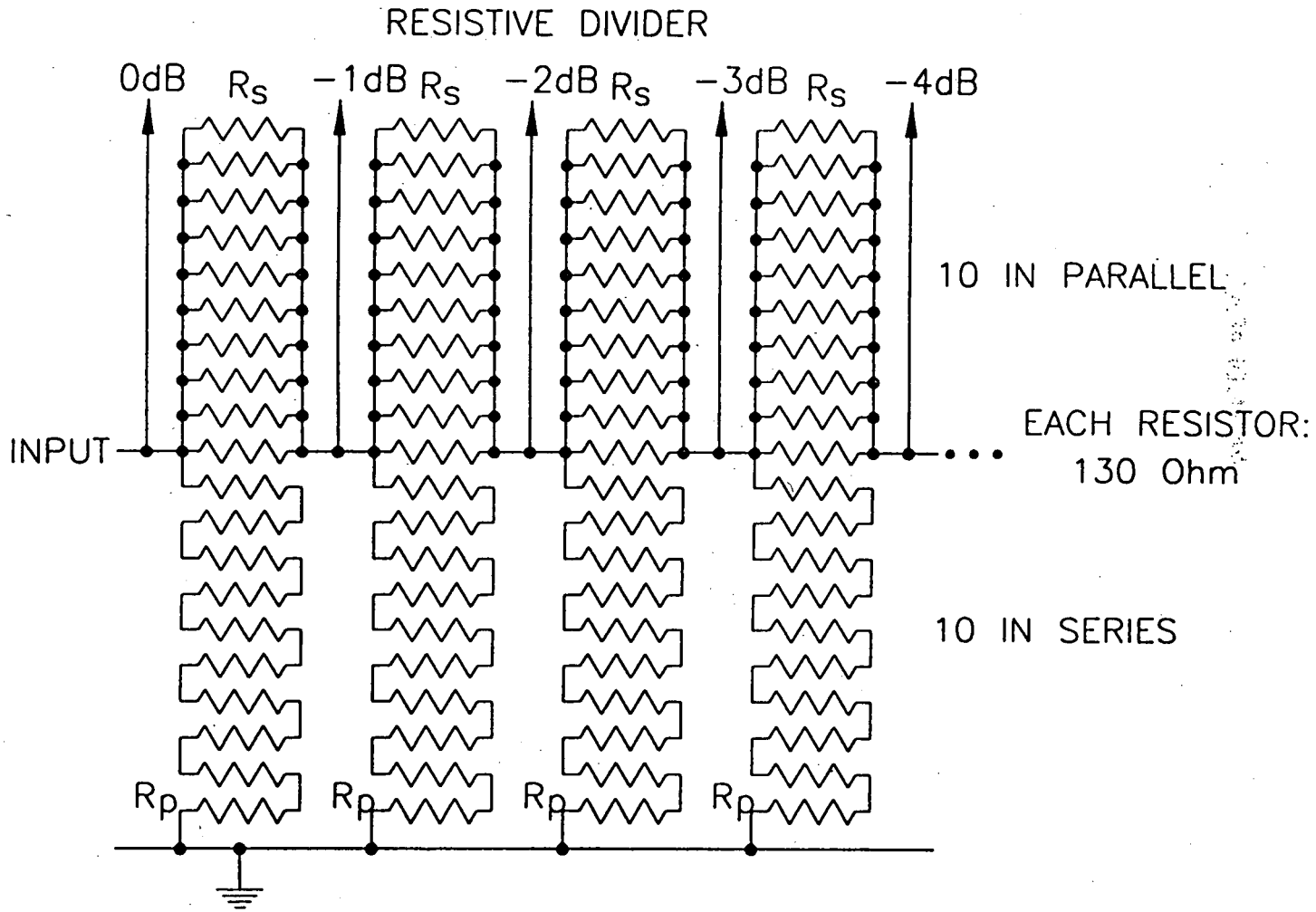


FIG.40



08270 2h6Gh0

FIG. 41



0082F0 2A6E6A60

FIG. 42

NON–MONOTONICITY

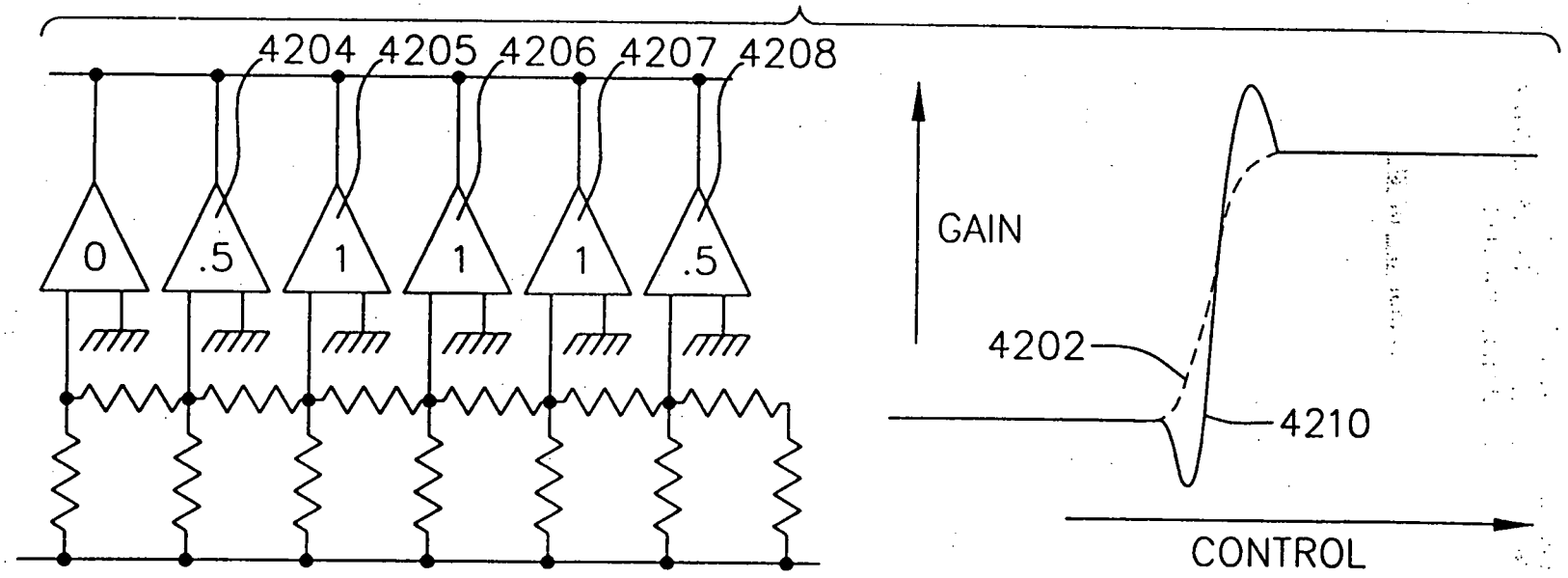
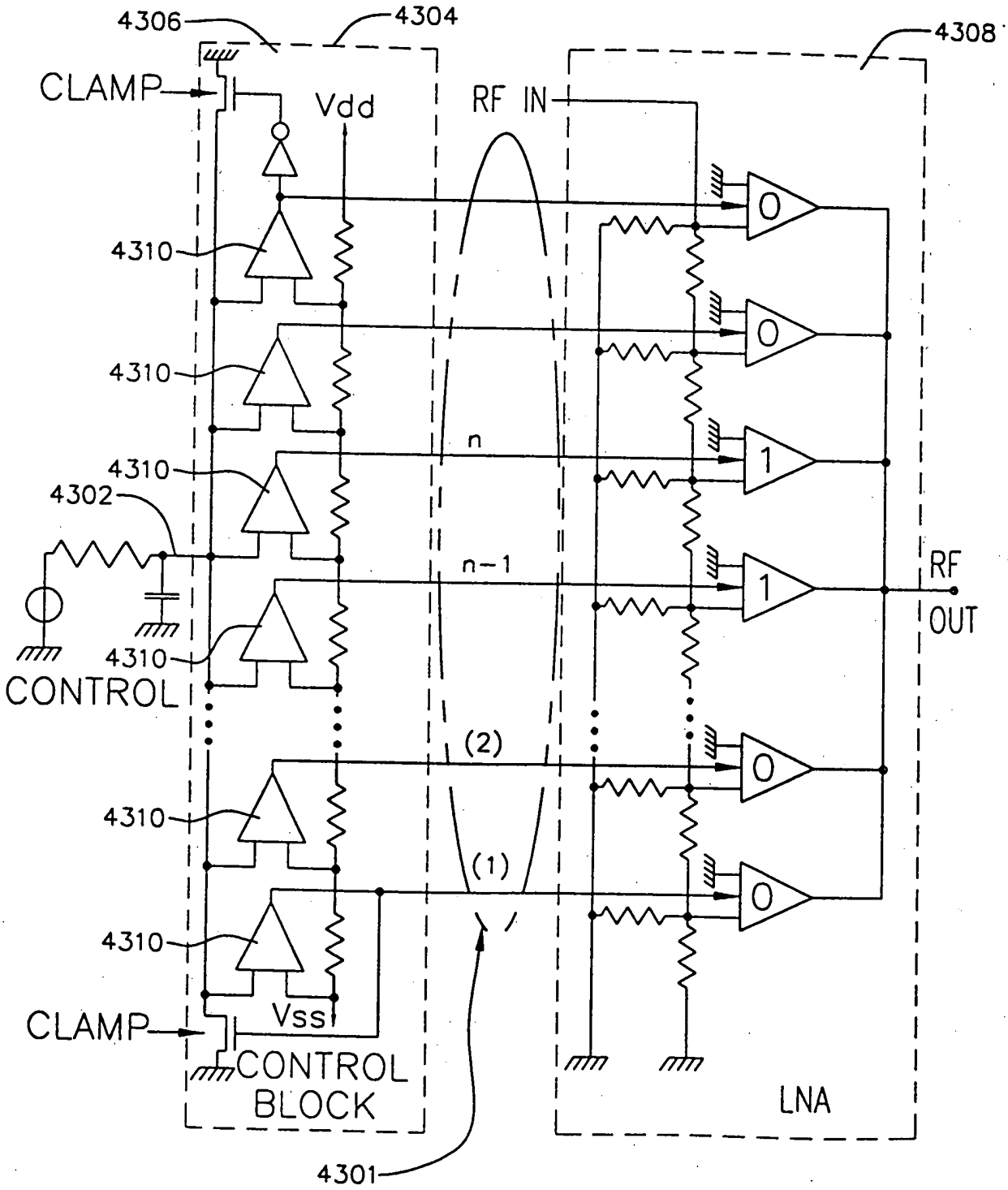


FIG.43

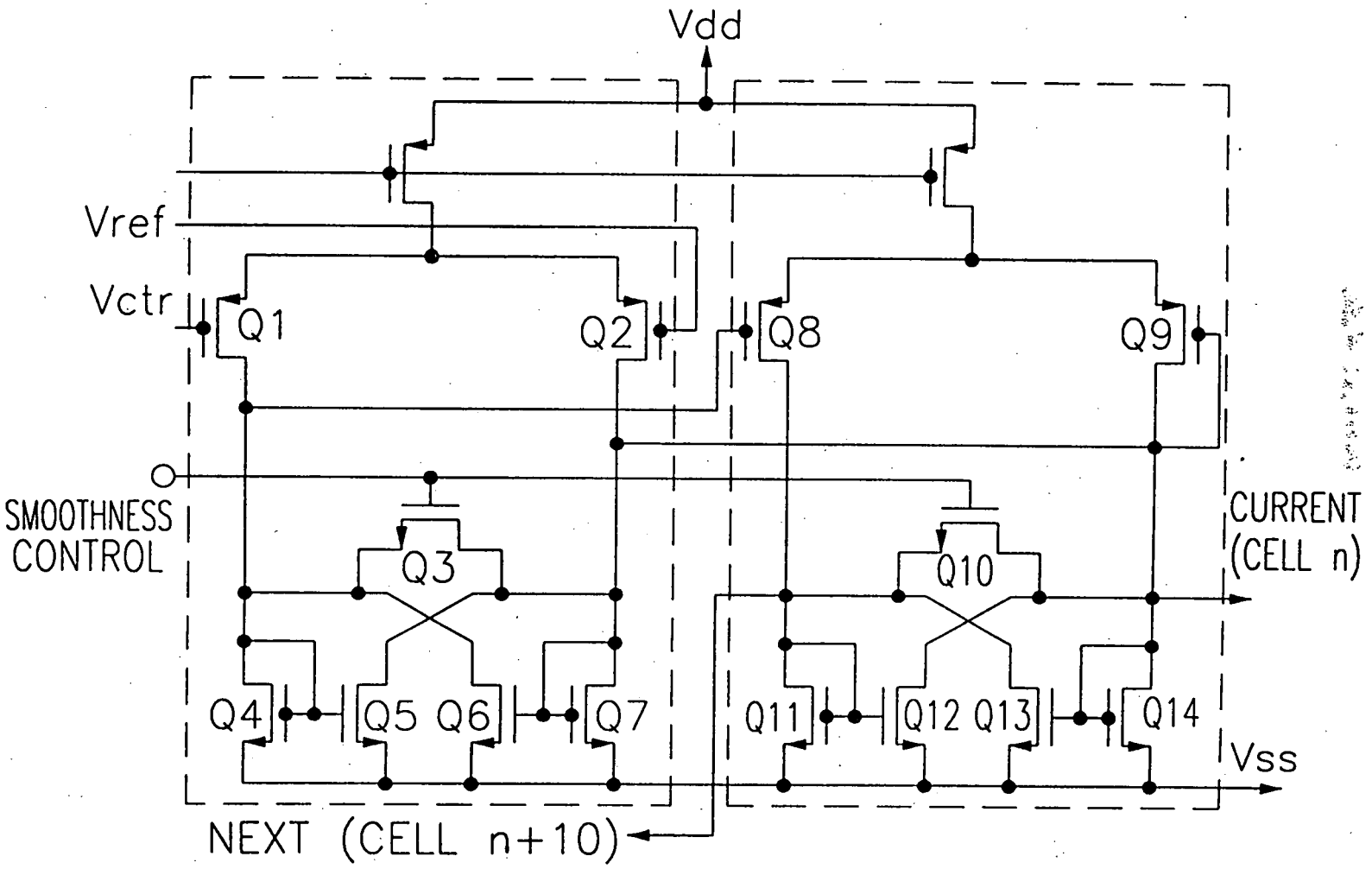
CLAMPING CONTROL RANGE



0082T0" 2h6E6h60

FIG. 44a

CONTROLLED GAIN COMPARATOR



08870 2H6260

FIG.44b

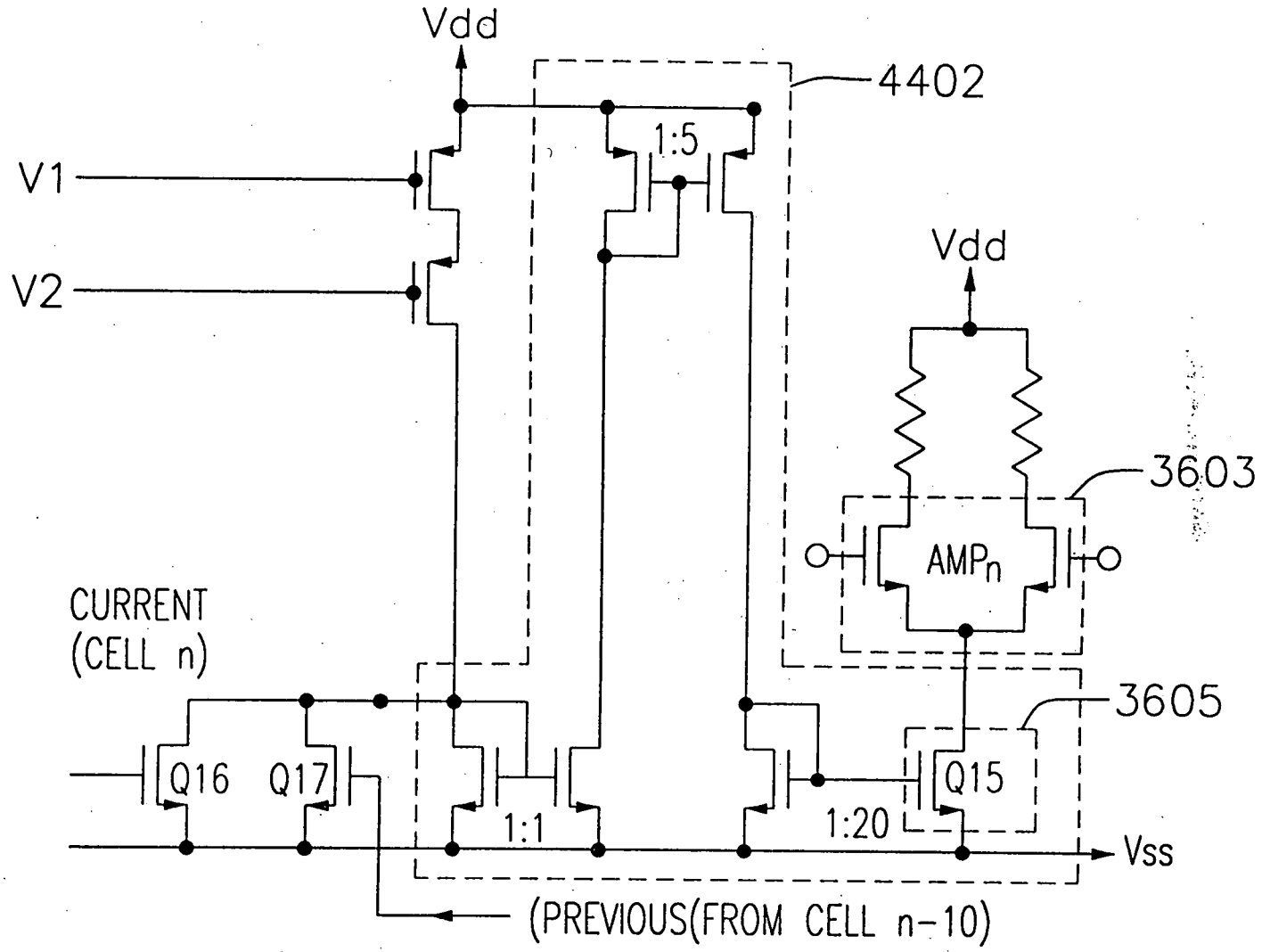
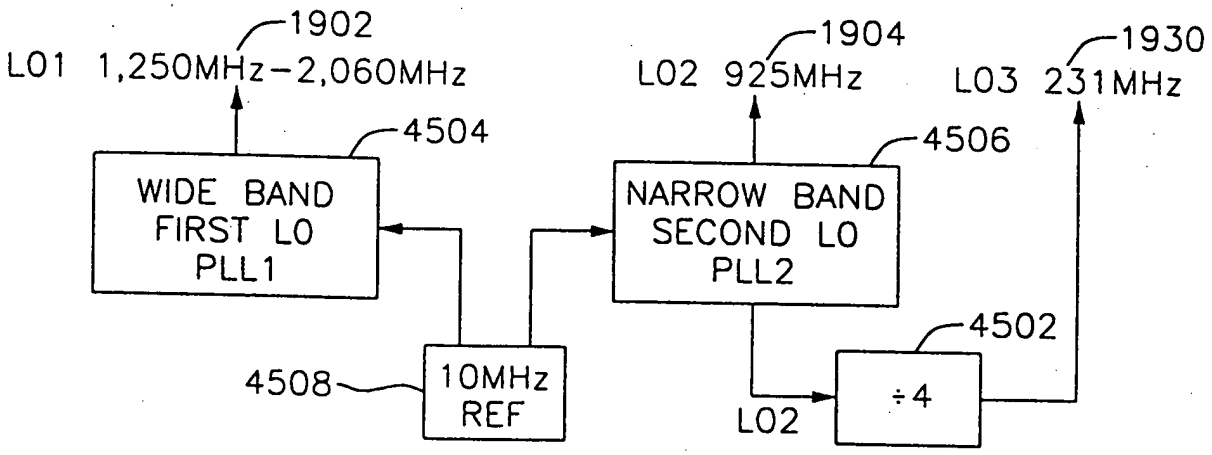
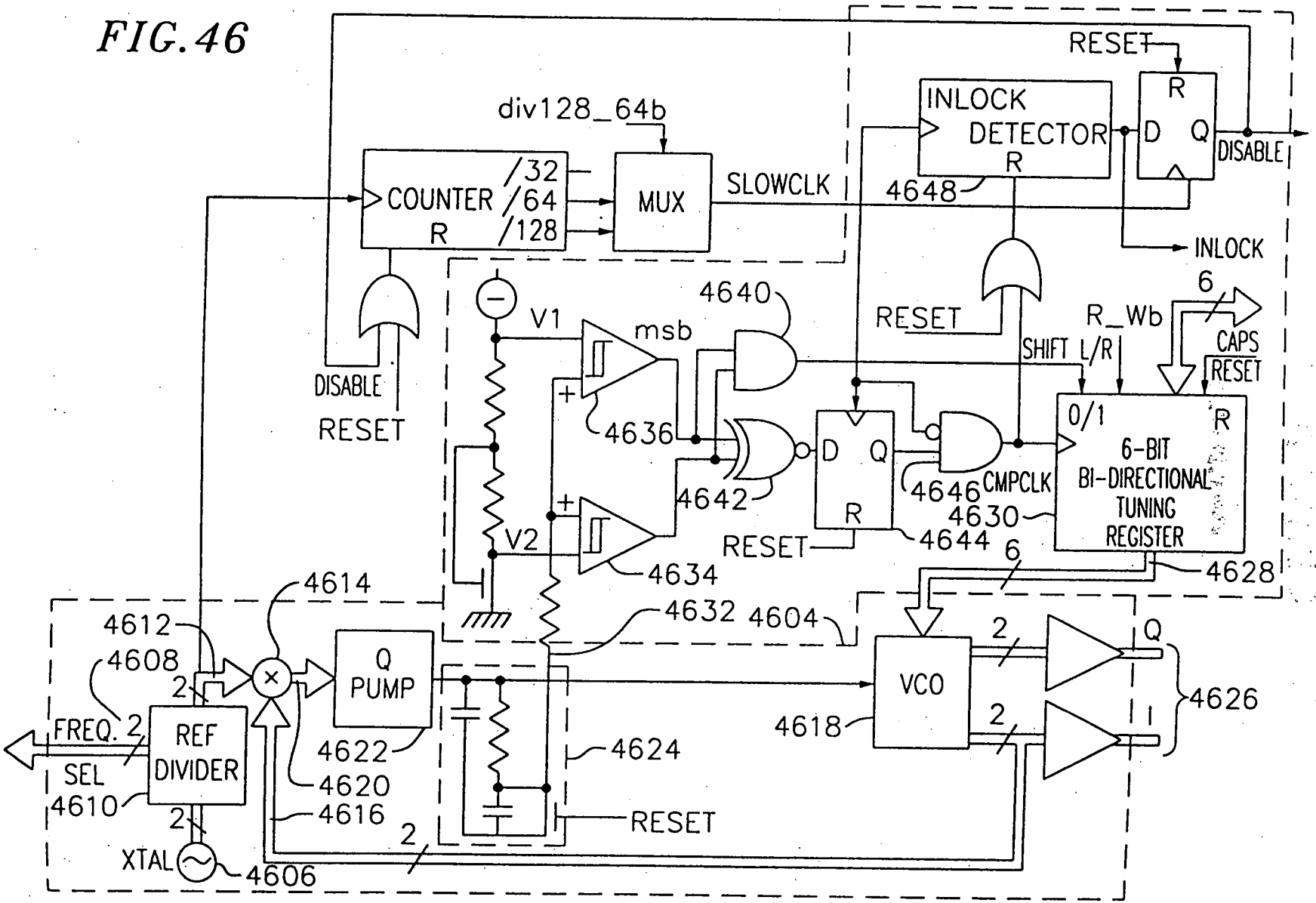


FIG.45


1902
LO1 1,250MHz–2,060MHz
1904
LO2 925MHz
1930
LO3 231MHz
4504
WIDE BAND
FIRST LO
PLL1
4506
NARROW BAND
SECOND LO
PLL2
4502
÷4
LO2
4508
10MHz
REF

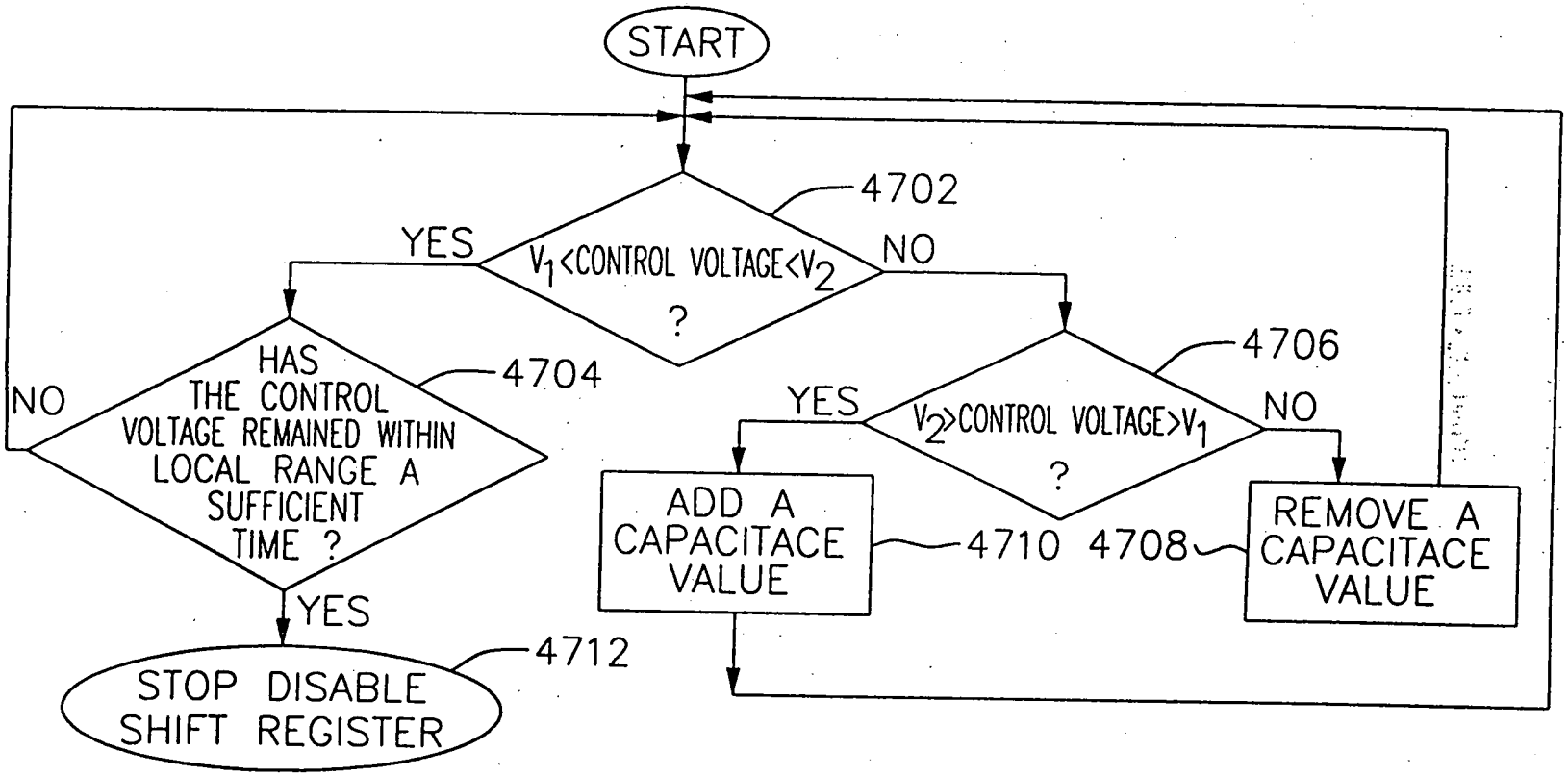
08270 2n62n60

FIG. 46



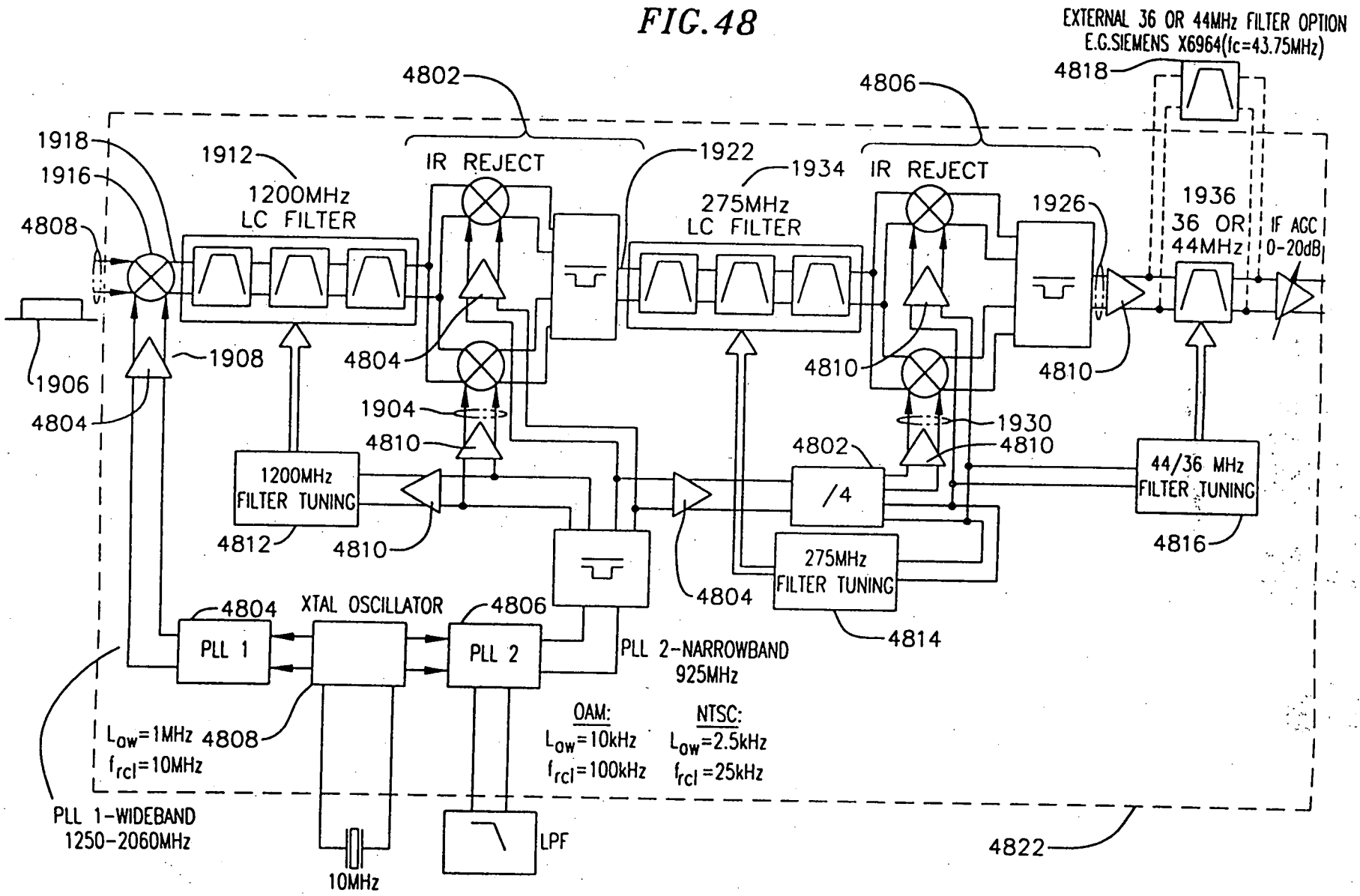
08270 "26260

FIG. 47



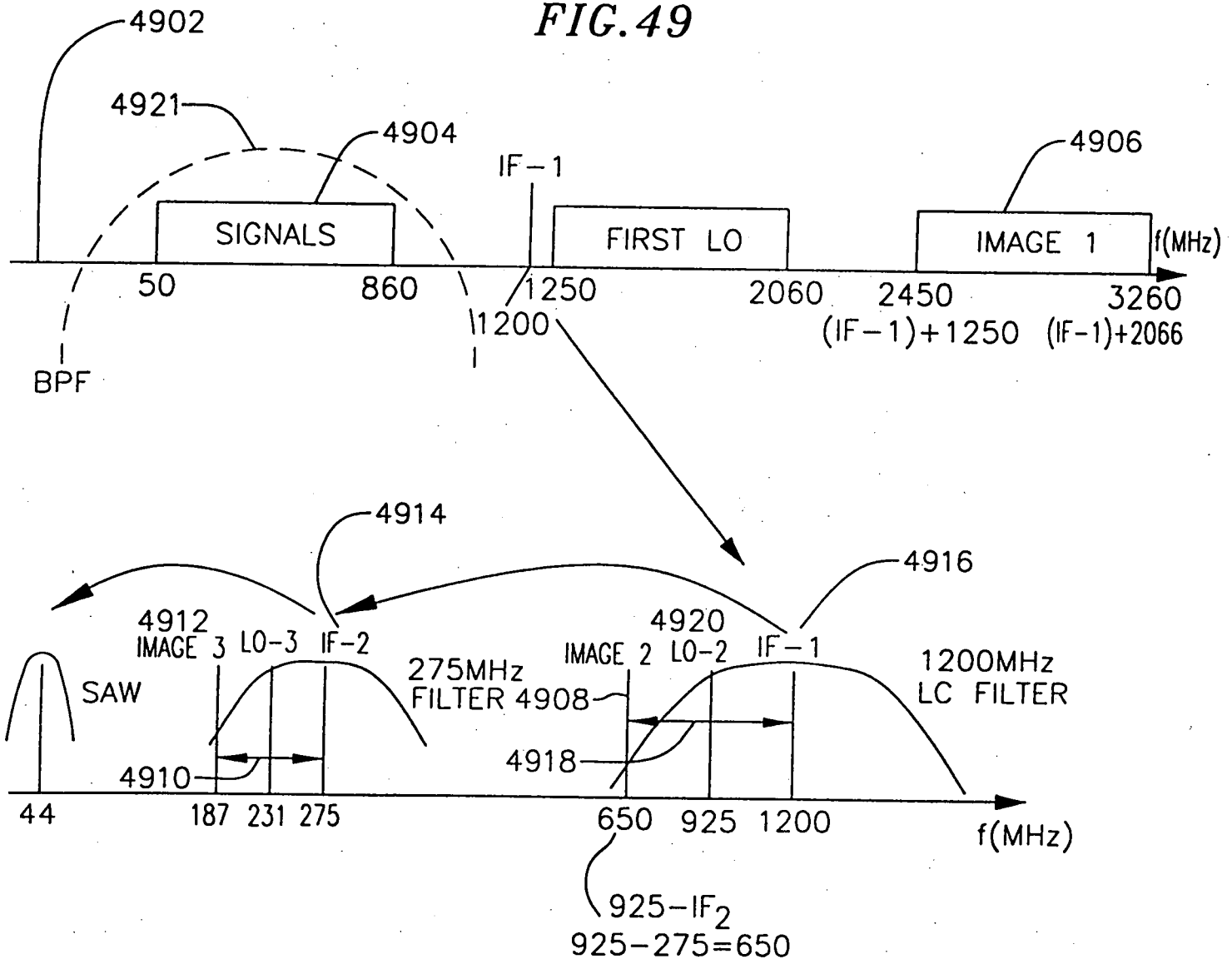
US 6,826,160

FIG. 48



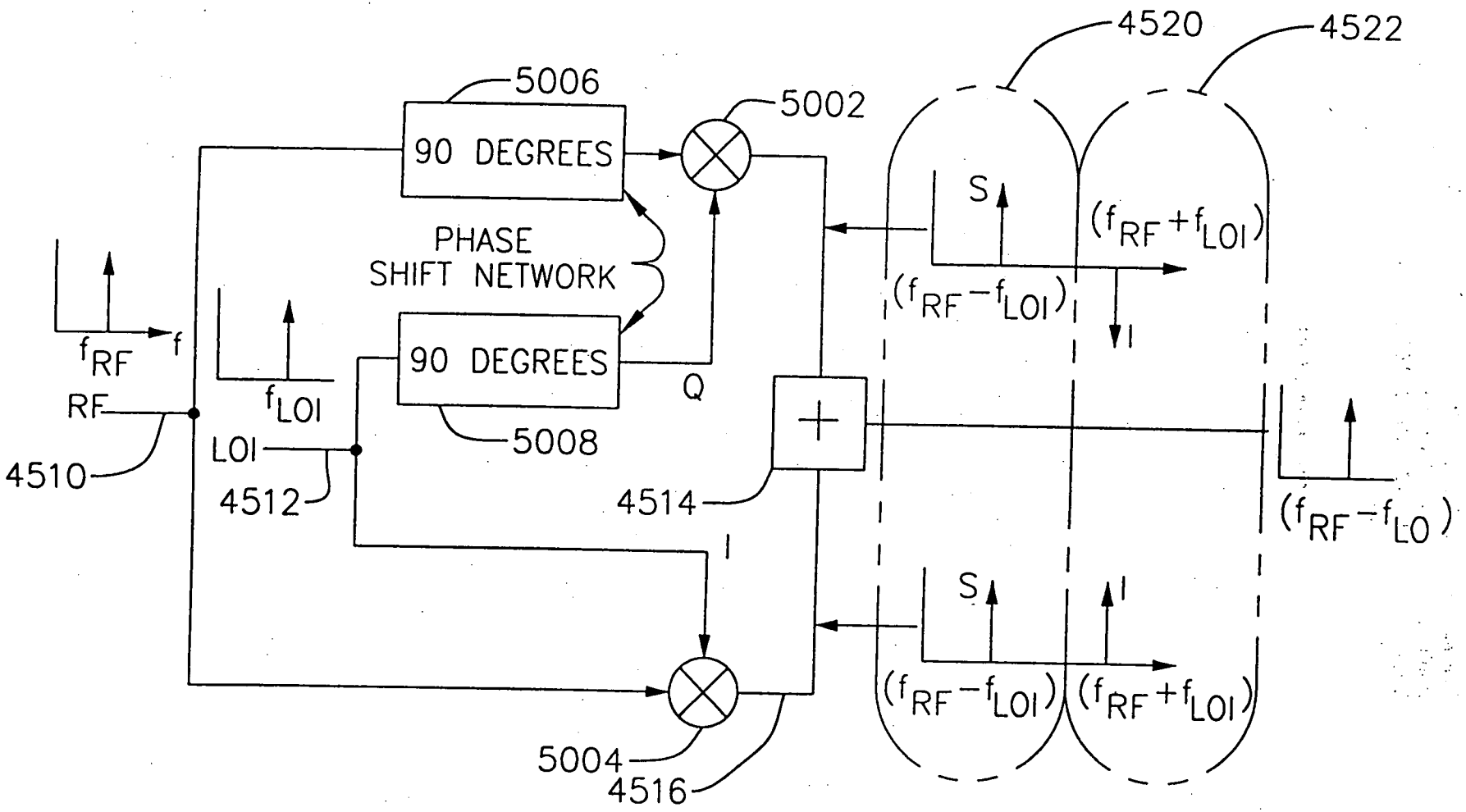
0820'2666660

FIG. 49



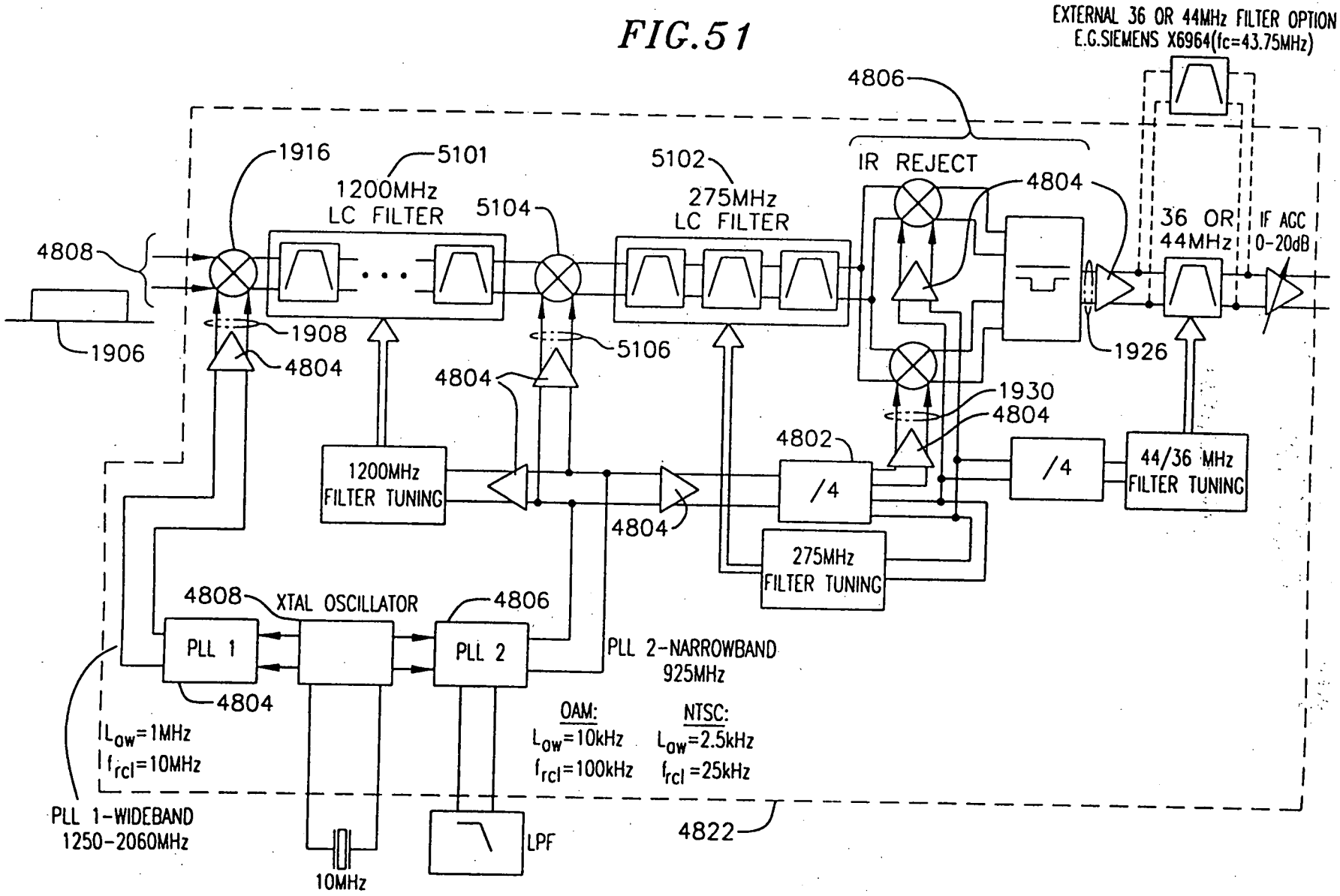
0082T0' 2h6E6h60

FIG.50



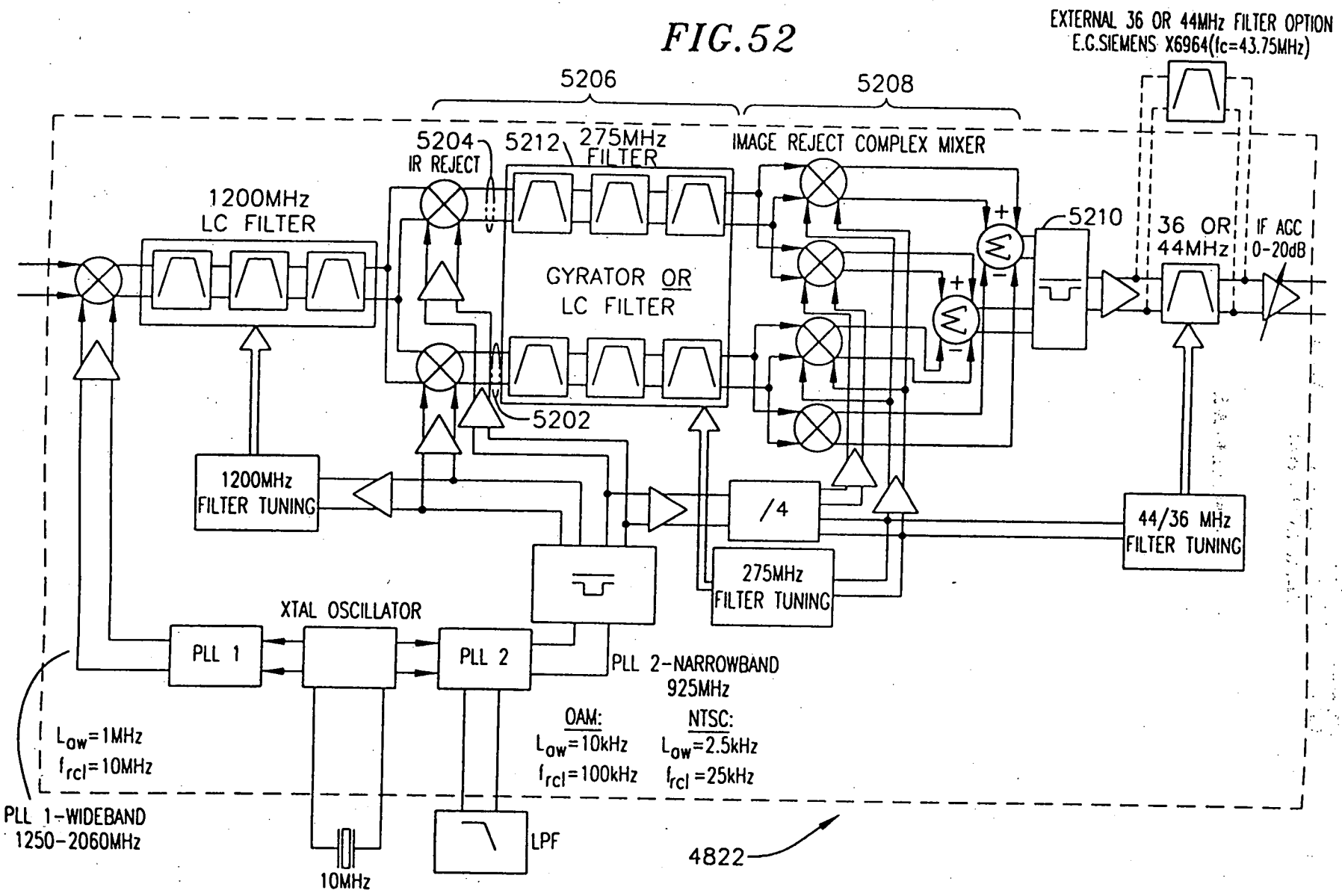
08270 2606

FIG.51



Doc ID: 8166160

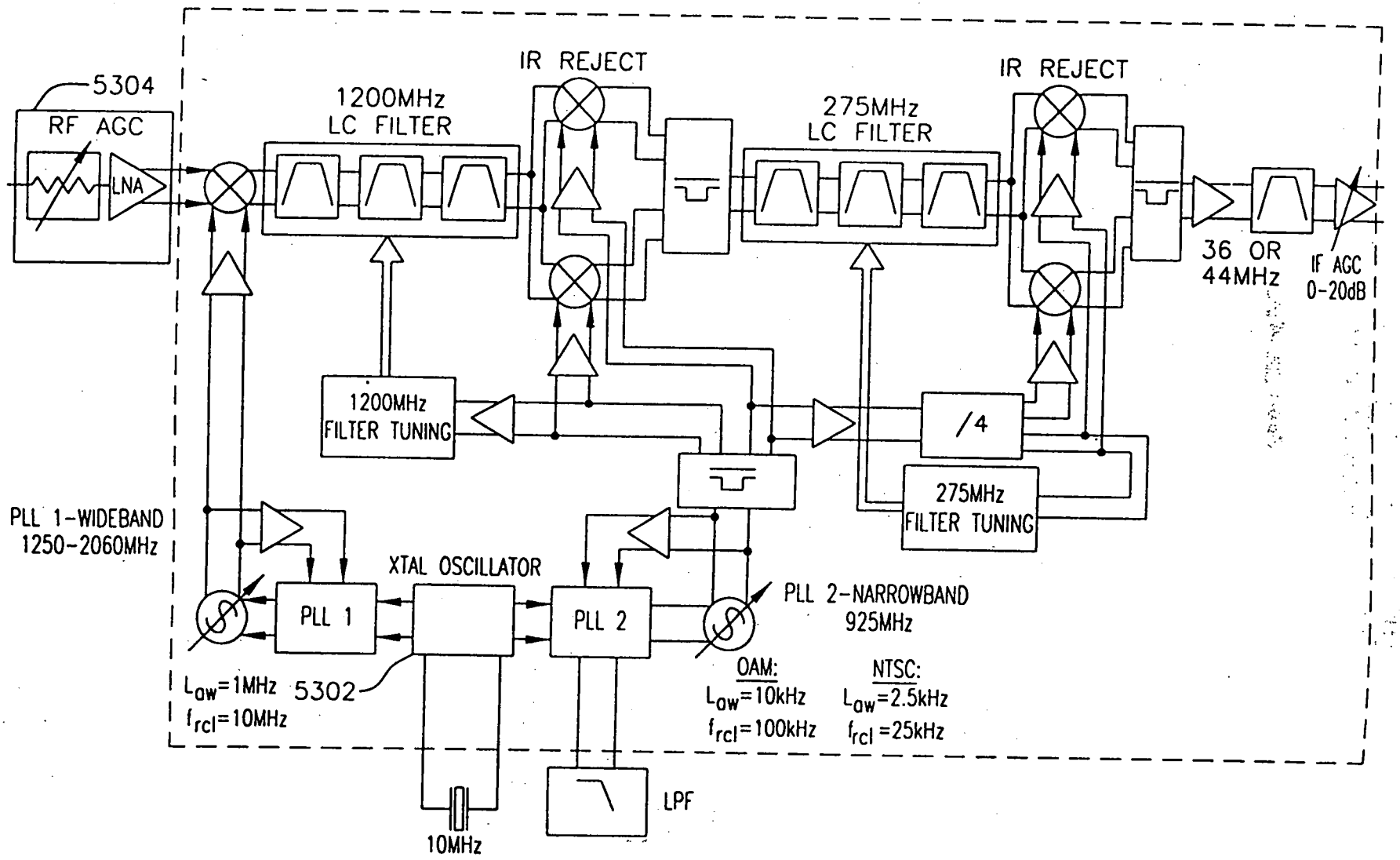
FIG. 52



08270 "26080

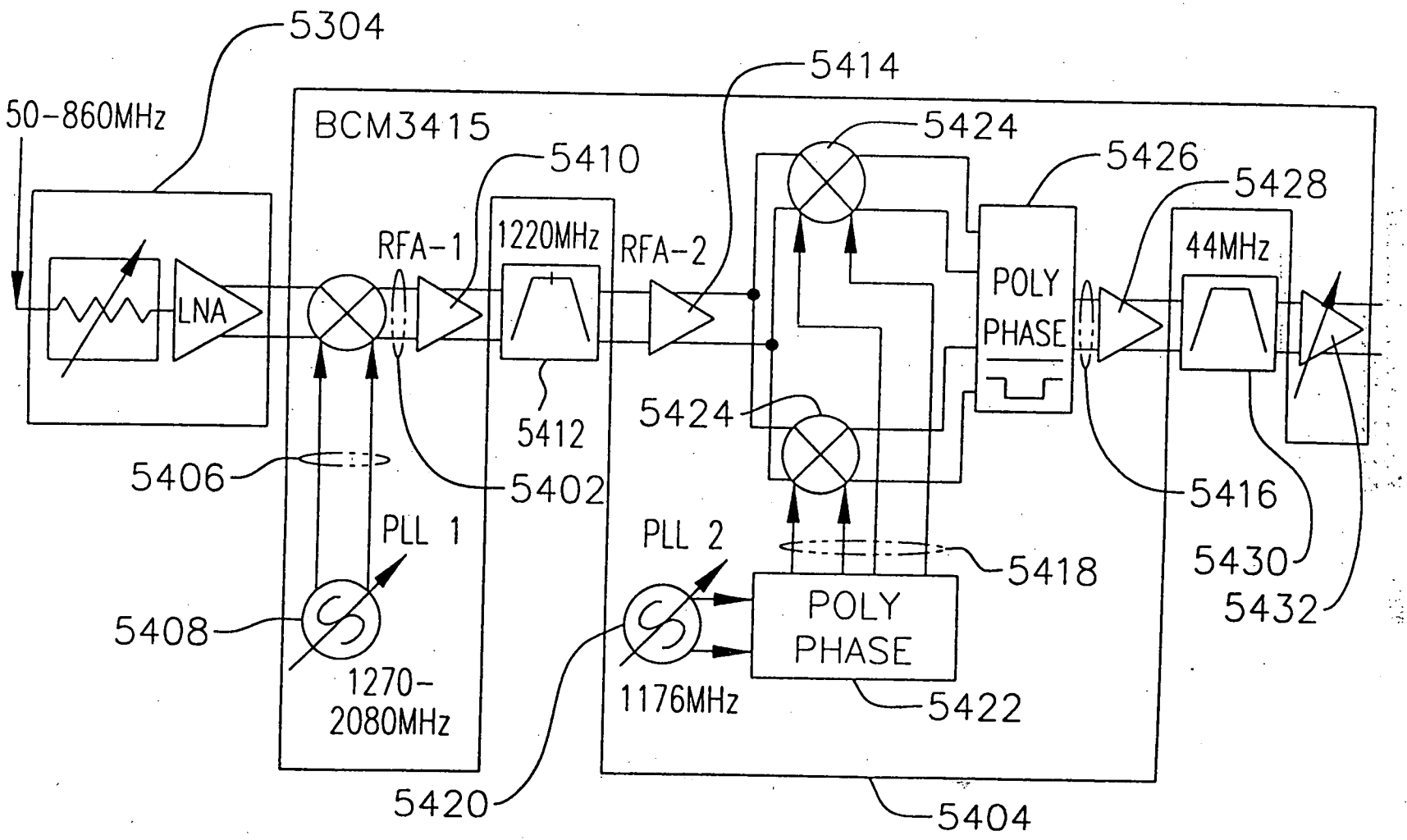
FIG.53

CATV TUNER



Gobetz Exhibit

FIG.54



08210 2626D

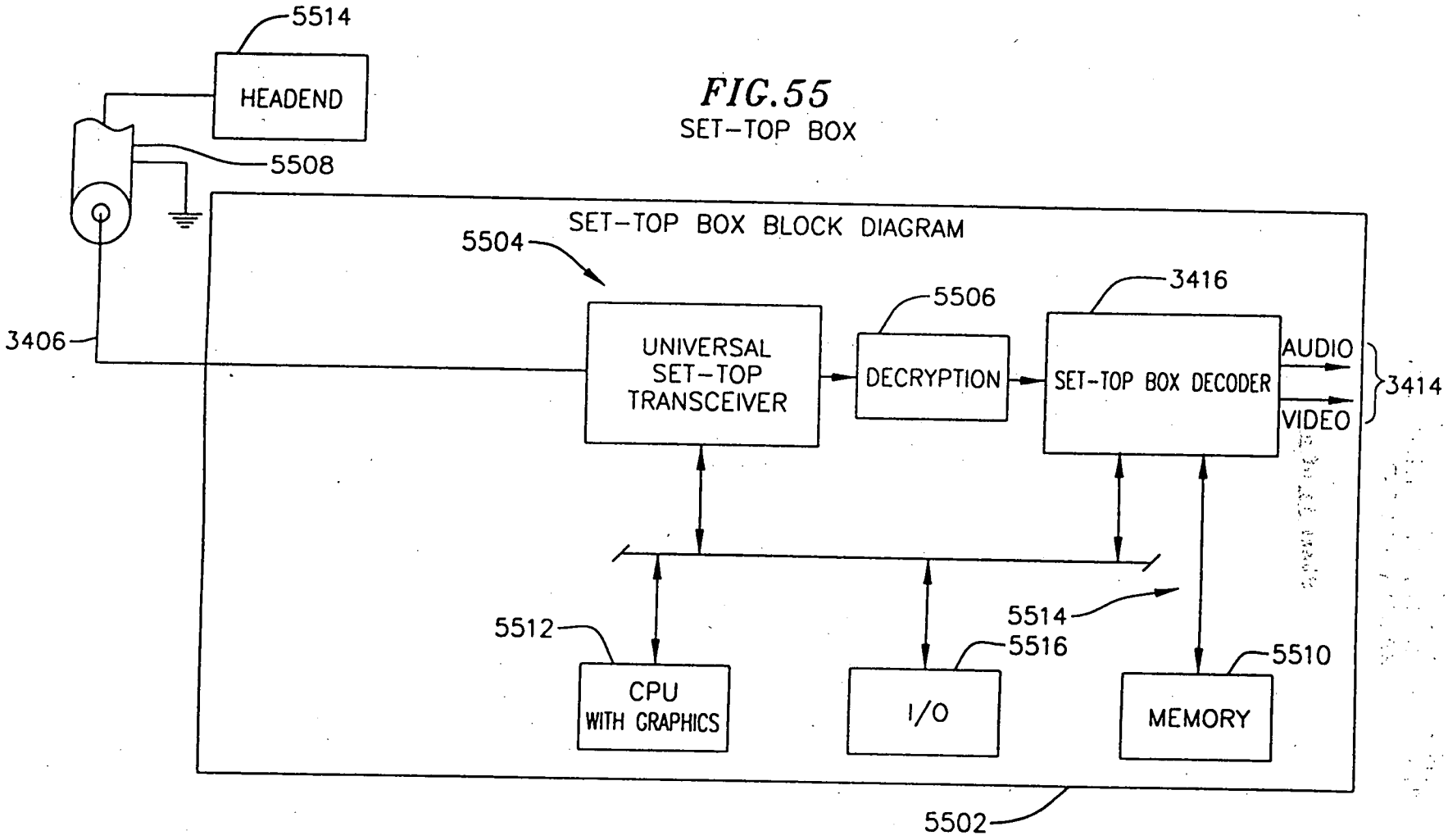
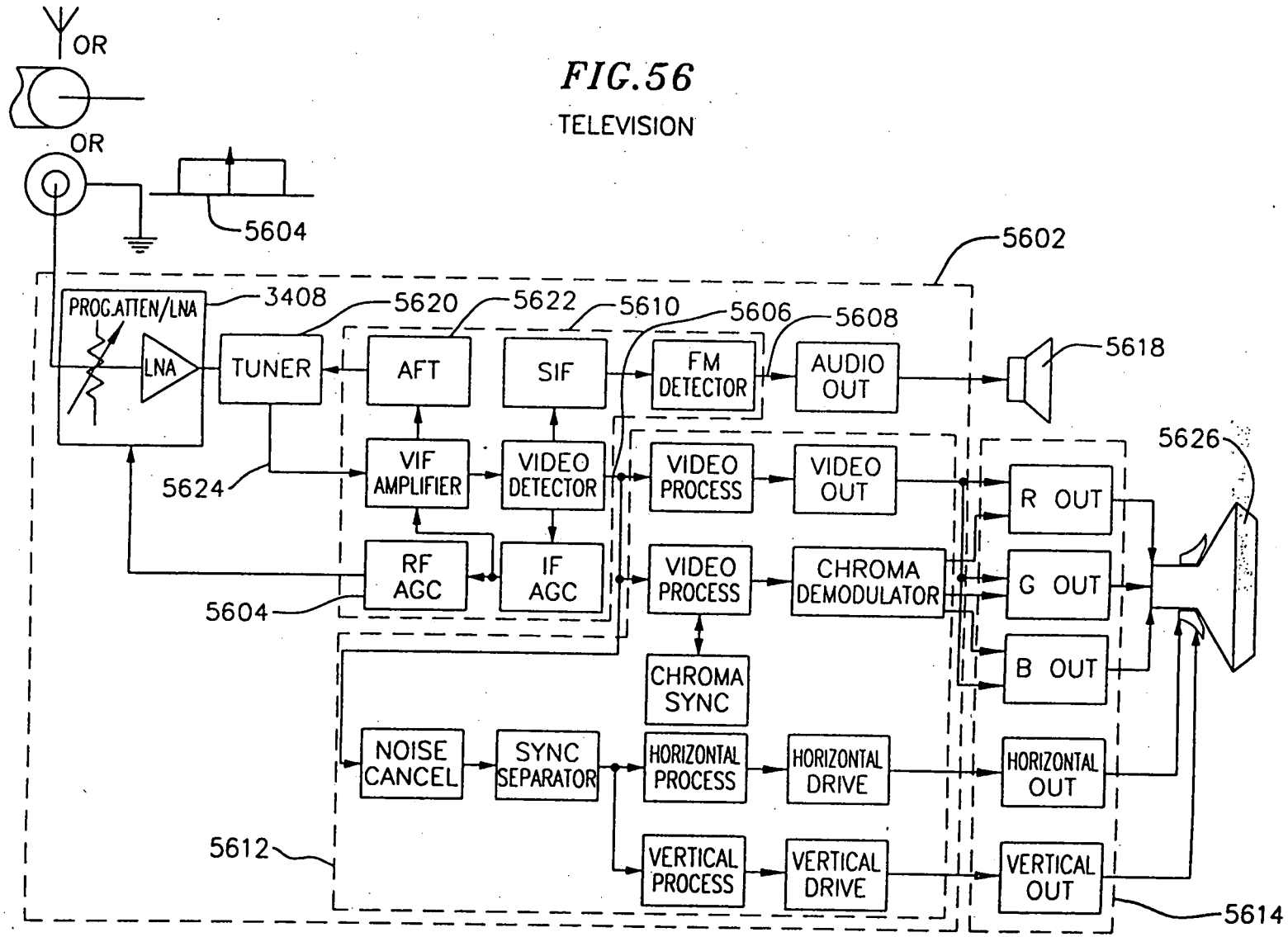


FIG.55
SET-TOP BOX

08670 2H6E6H60

FIG.56

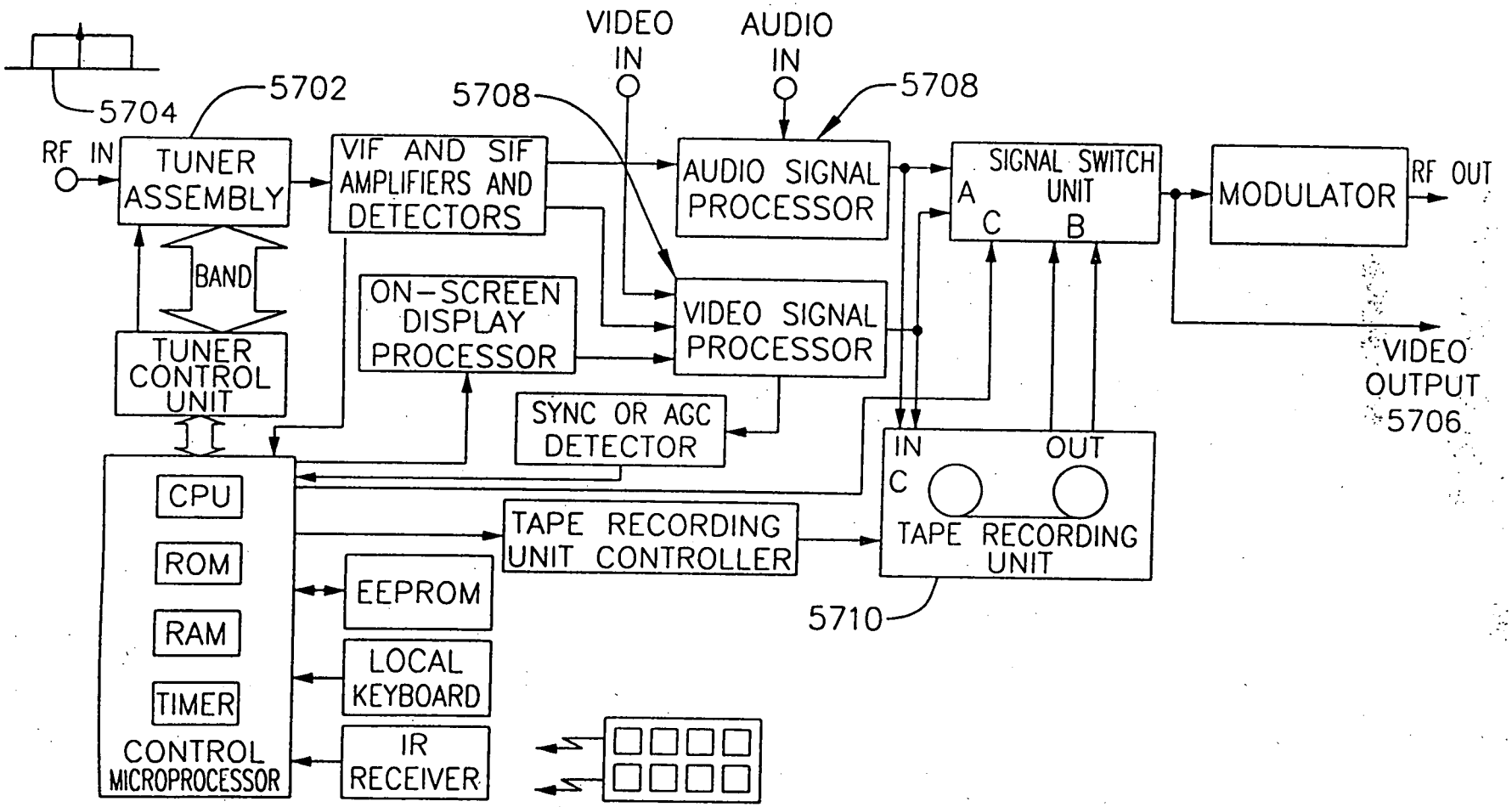
TELEVISION



08270 26660

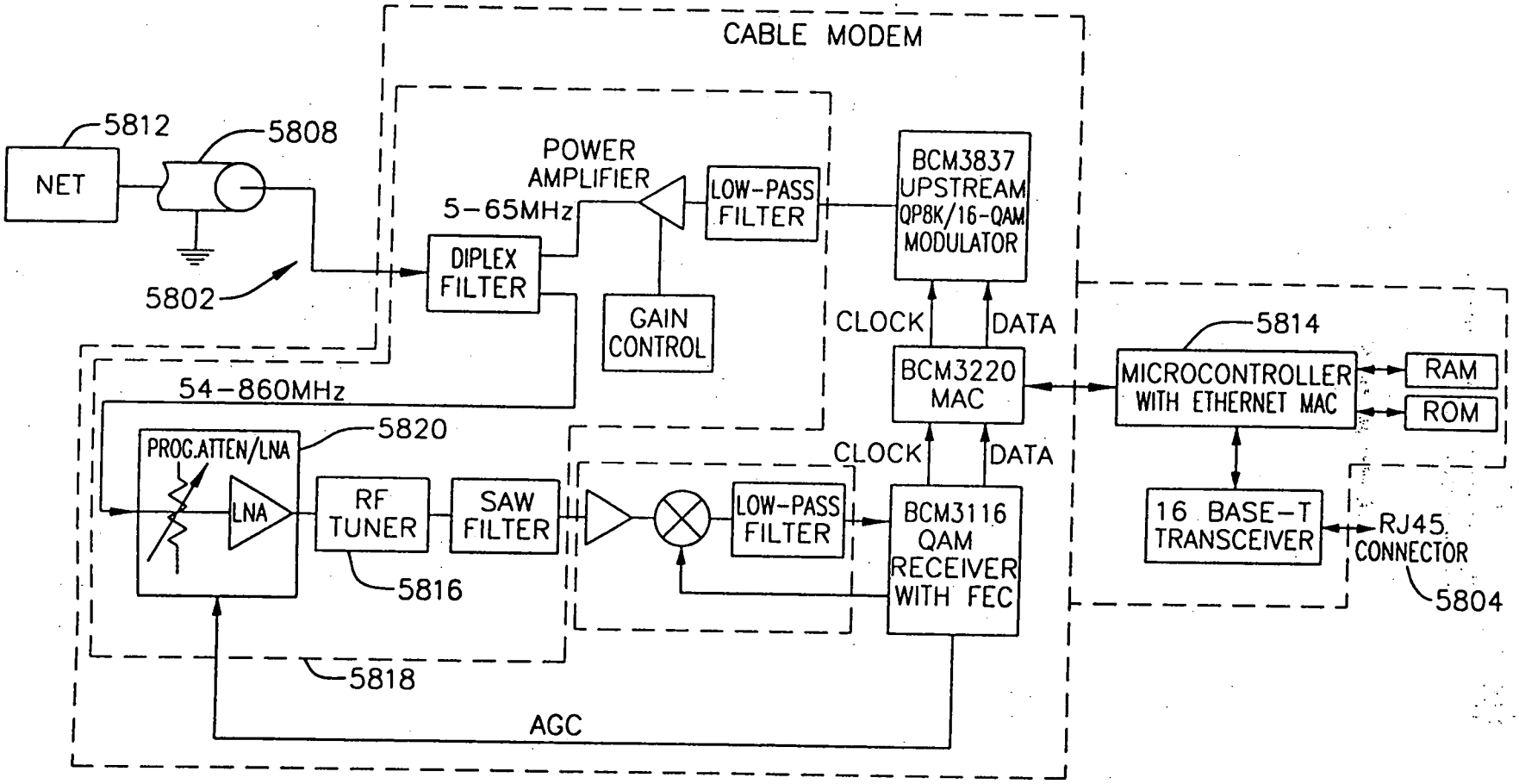
FIG.57

VCR BLOCK DIAGRAM



08870 2h6E6h60

FIG.58



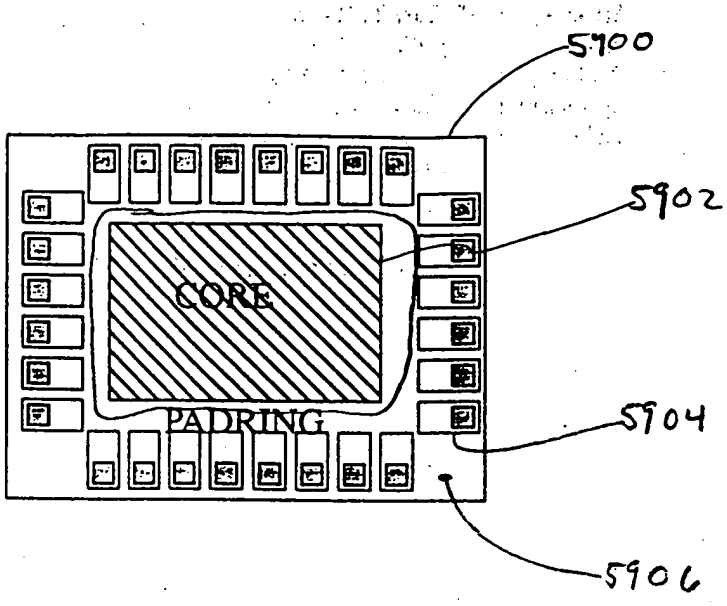

5900
5902
CORE
PADRING
5904
5906

FIG 59

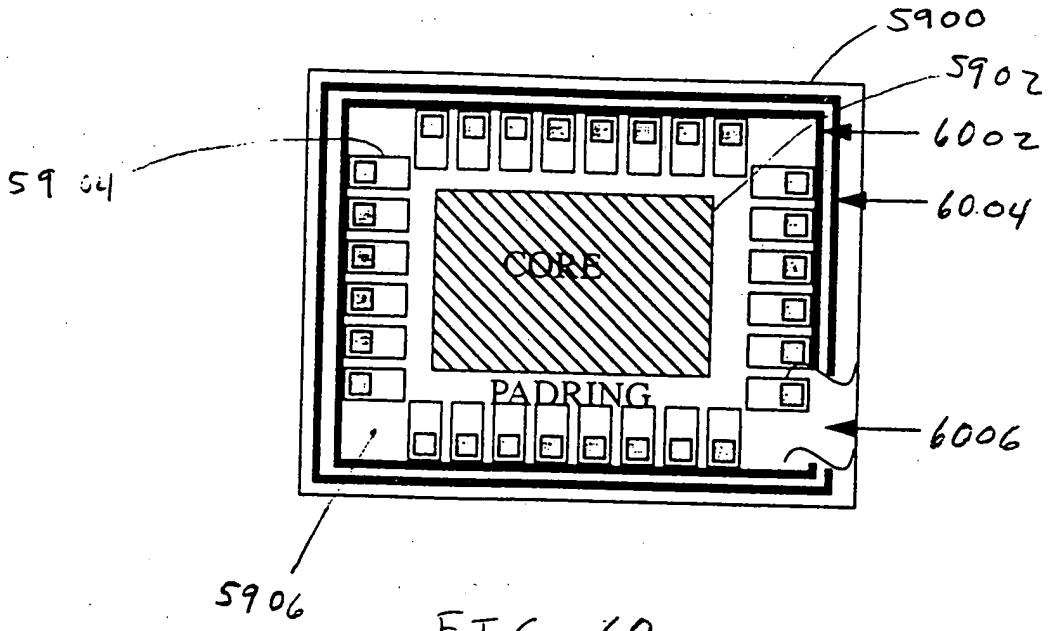

5900
5902
6002
6004
5904
CORE
PADRING
6006
5906

FIG 60

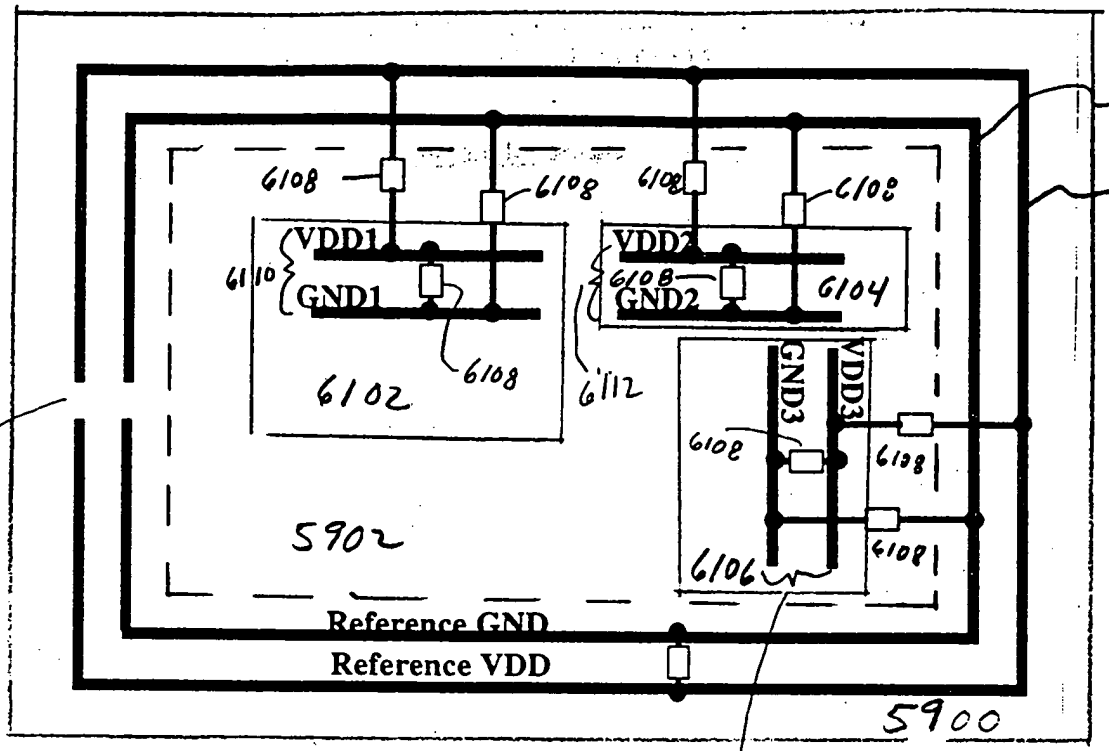

6002
GND
6004
VDD
6108
6108
6108
6108
VDD1
GND1
6110
6102
6108
6112
VDD2
GND2
6104
GND3
VDD3
6108
6108
6108
6106
6006
5902
Reference GND
Reference VDD
5900
6114

FIG 6.1

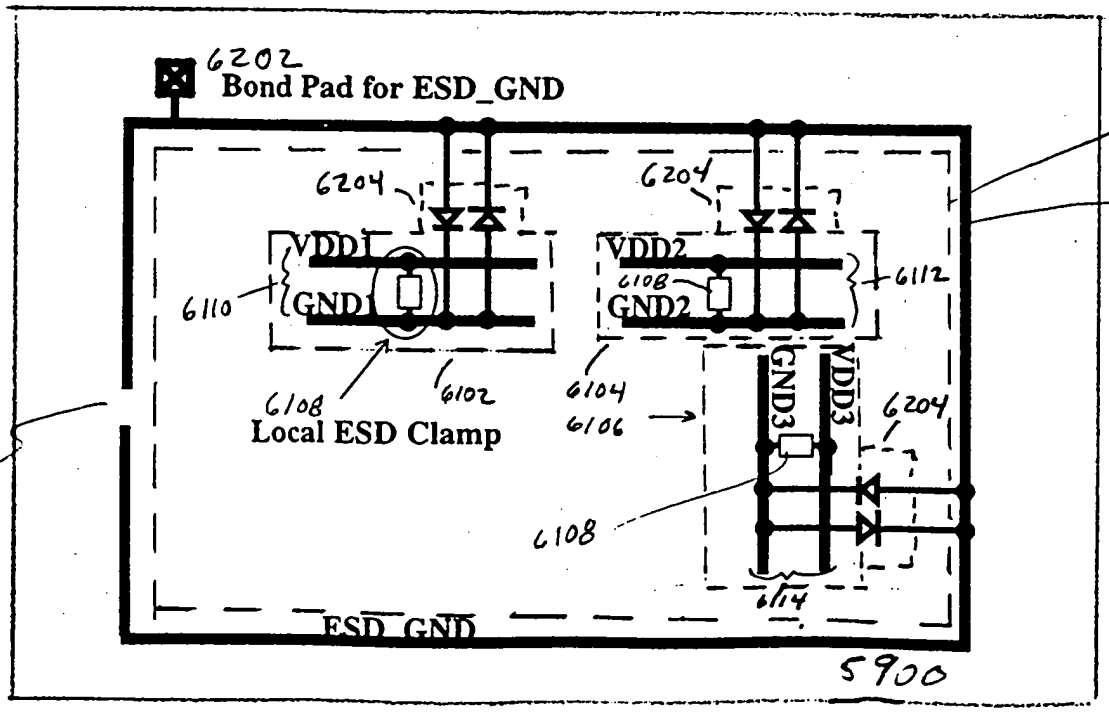

6202
Bond Pad for ESD_GND
5902
6200
6204
6204
VDD1
GND1
6110
VDD2
6108
GND2
6112
6108
6102
6104
6106
Local ESD Clamp
GND3
VDD3
6204
6108
6114
6006
ESD_GND
5900

FIG 6.2

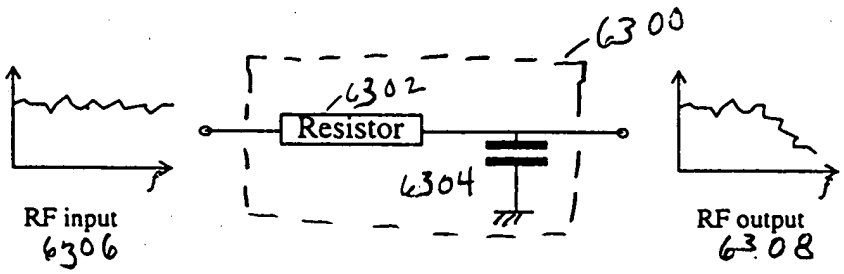


FIG 63

Adobe PDF Scanned

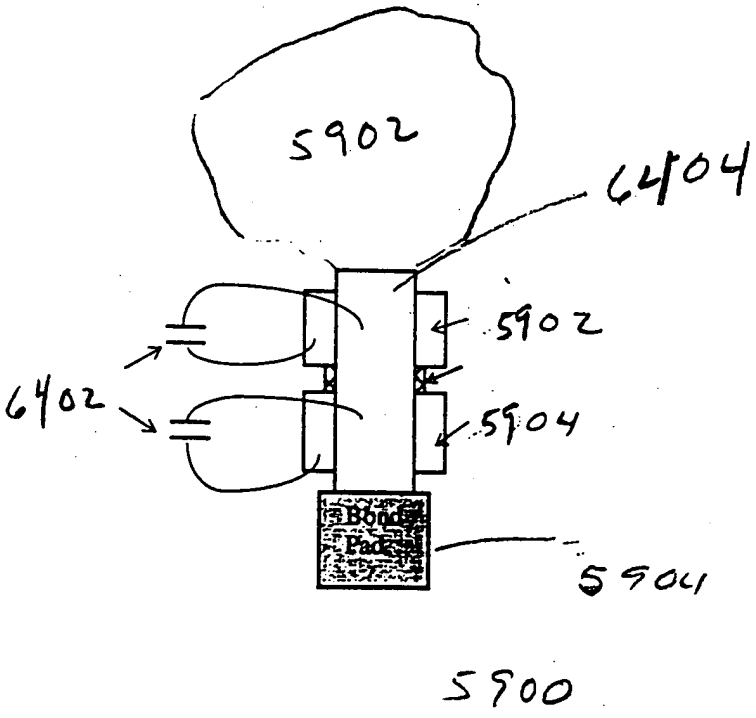


FIG 64

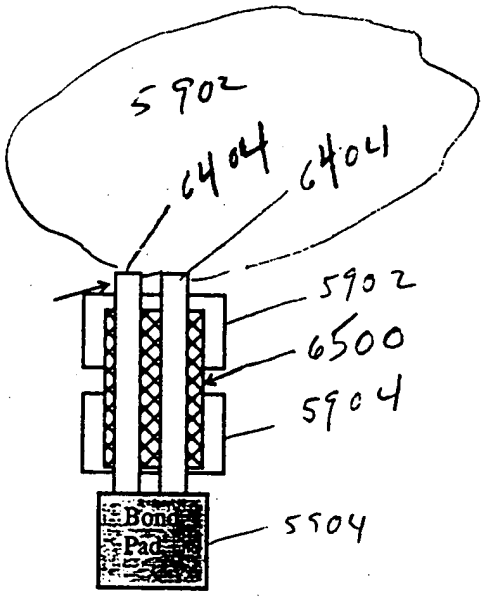


FIG 5

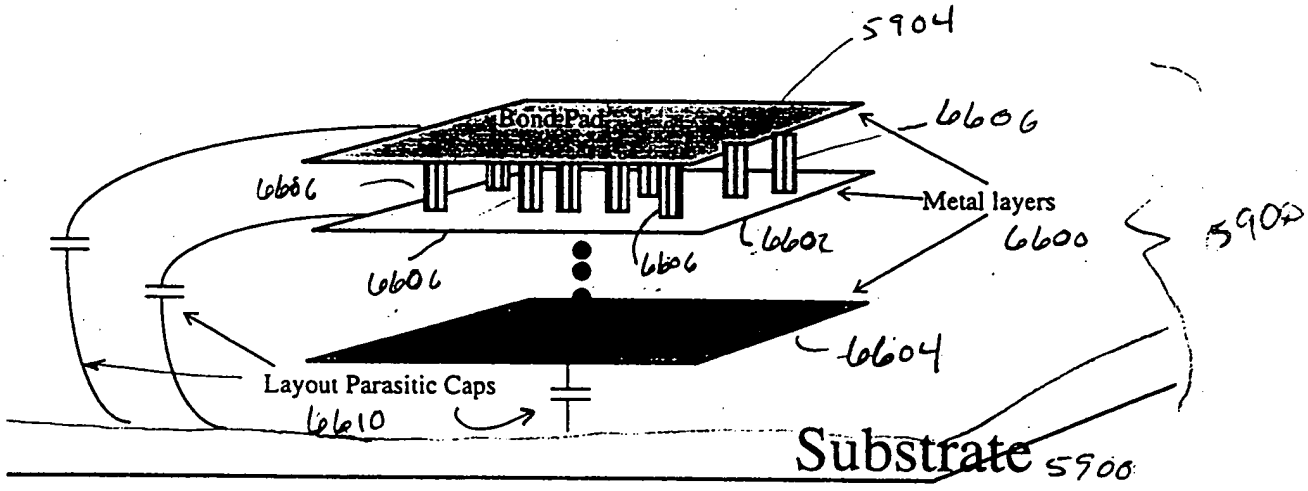

5904
Bond Pad
66006
6606
Metal layers
66002
6606
6606
66000
5902
66004
Layout Parasitic Caps
66010
Substrate
5900

FIG_66

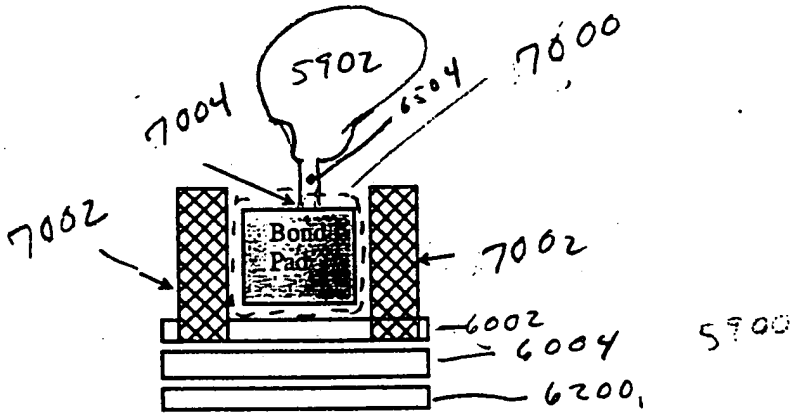


FIG. 67

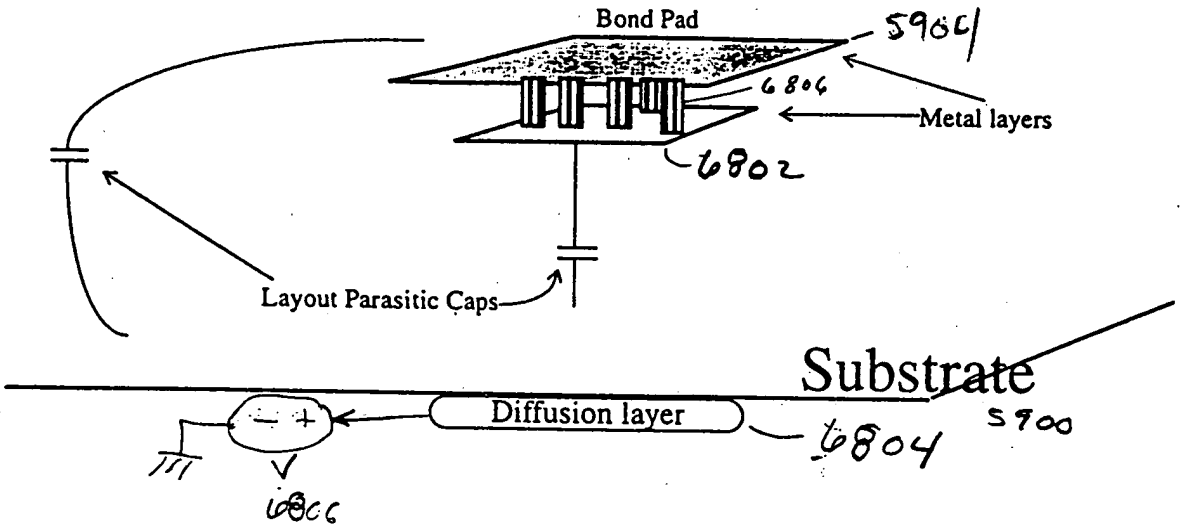
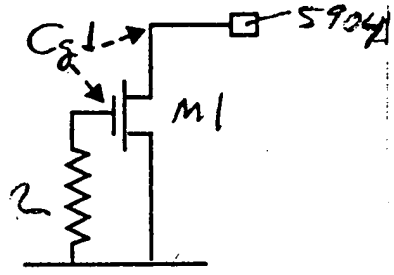
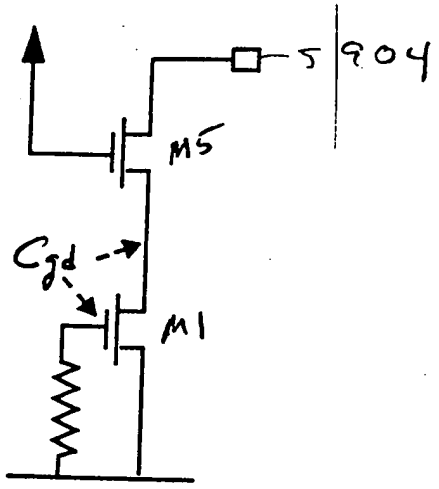

Bond Pad
5906
6806
Metal layers
6802
Layout Parasitic Caps
Substrate
5900
Diffusion layer
6804
6808

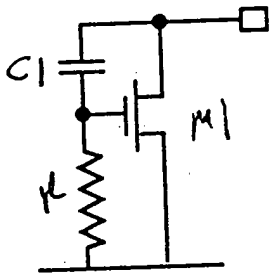
FIG. 68



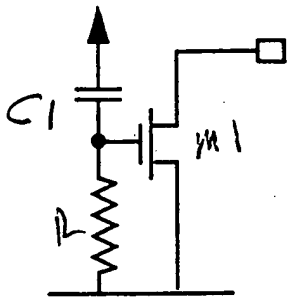
6902



6904

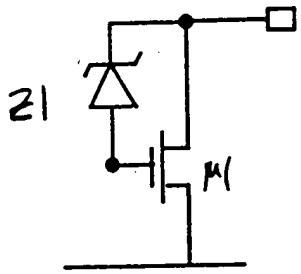


6906



6908

PRIOR ART



6910

FIG 69

DOCKET ENGINE

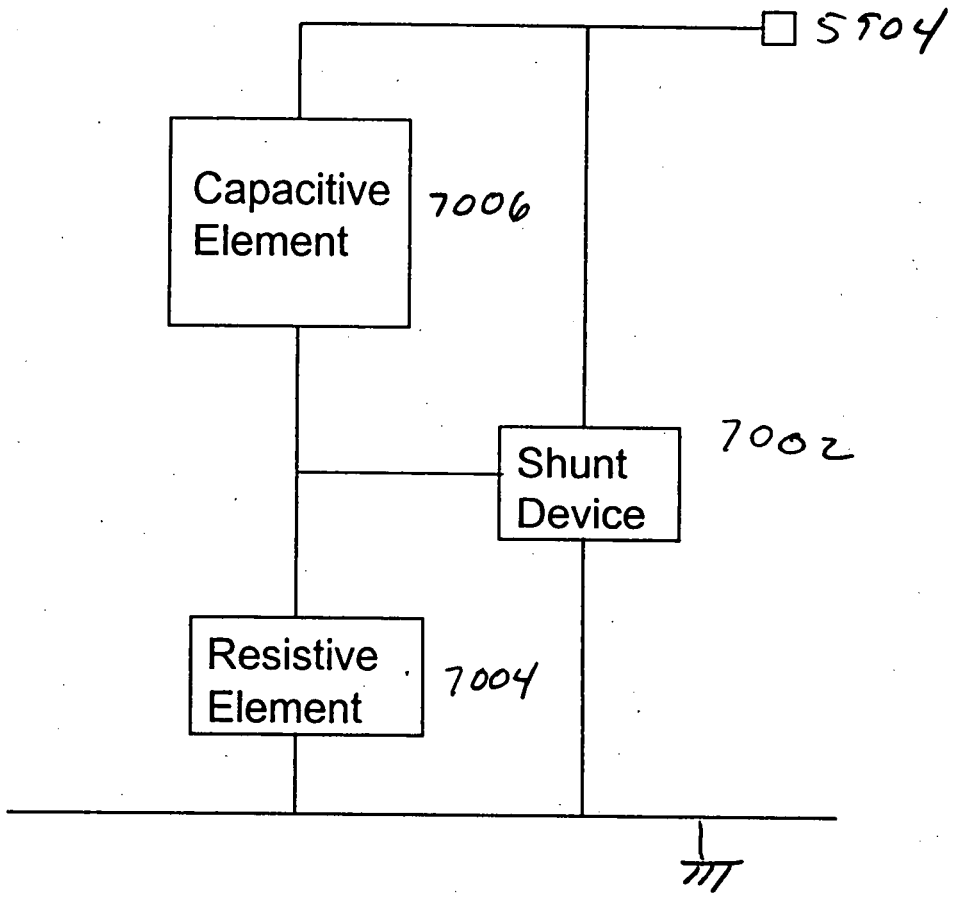


FIG. 70

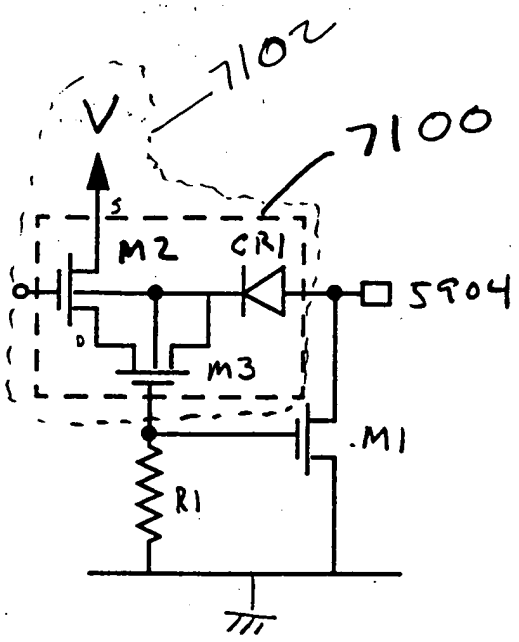


FIG. 7

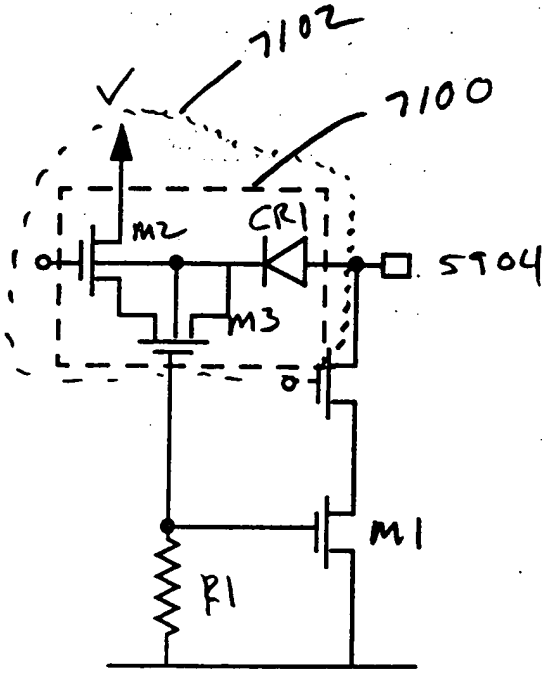


FIG. 72

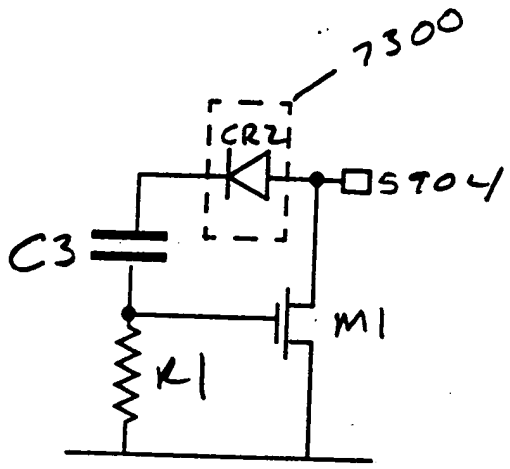


FIG. 73